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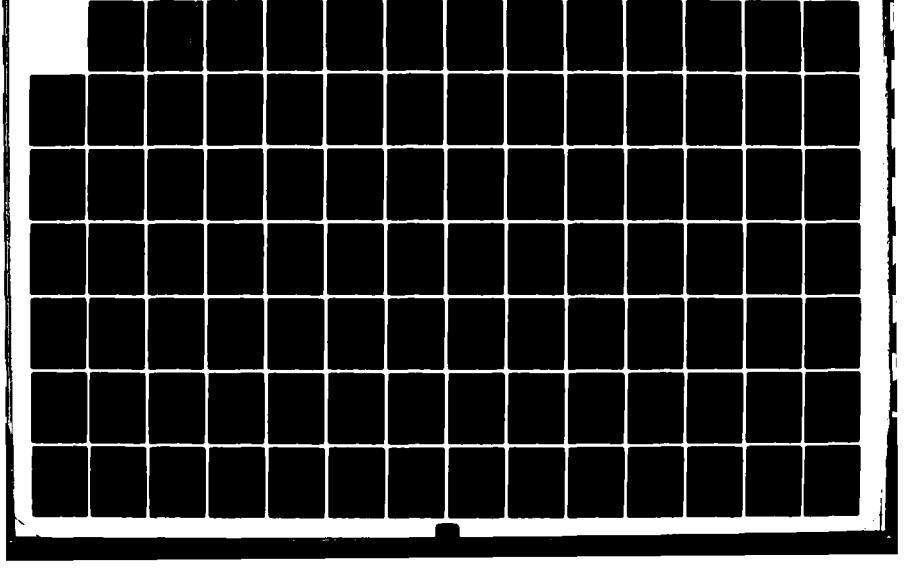

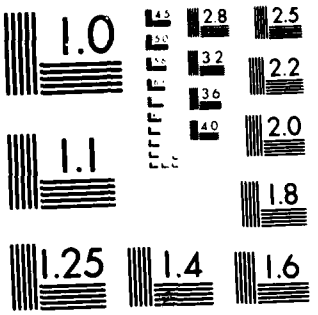

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ANNUAL TECHNICAL REPORT
(FOR PERIOD: JUNE 11, 1982 TO JUNE 10,1983)

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STUDY OF DEEP-LEVEL DEFECTS AND TRANSPORT PROPERTIES VS GROWTH PARAMETERS AND ANNEALING CONDITIONS IN III-V COMPOUND SEMICONDUCTORS

by

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GaAs, InP, LPE, MOCVD, LEC, grown-in defect, electron trap, hole trap, DLTS, C-V, I-V, trap density, defect energy level, emission rate, capture cross section, thermal annealing, laser annealing, one-MeV electron irradiation, electron flux, electron fluence, Hall effect, resistivity, electron mobility, vacancy, antisite defect, III-V compound semiconductors.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objectives of this research program are: (1) To investigate the grown-in defects and the effects of thermal and laser annealing on the grown-in defects in LEC grown Zn-doped InP, (2) to study the transport properties in n-type InP, (3) to characterize the grown-in defects vs annealing temperature in the LEC grown GaAs, and compare the deep-level defects in the MOCVD grown GaAs on semi-insulating GaAs- and Ge- substrates, (4) to study the one-MeV electron radiation induced deep level defects in LPE grown GaAs and the effects of thermal annealing on these defects. Deep-level Transient Spectroscopy (DLTS)

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Capacitance-Voltage (C-V), Current-Voltage (I-V), Resistivity, and Hall effect measurements were employed to study the deep-level defects and transport properties vs growth parameters and annealing conditions in GaAs and InP specimens. The main technical findings are summarized as follows:
(1) For the LEC grown Zn-doped InP, Schottky barrier diodes using Ag, Au, and Al contacts were fabricated for the DLTS and the C-V measurements. A grown - in hole trap with energy of Ev + 0.52 eV and density of 1.5 x 10^{15} cm^{-3} was observed in all the samples studied here. Thermal annealing performed at 170°C for 32 hours yields a defect annealing rate of 0.025 per hour for this hole trap. A significant reduction in the density of this hole trap was also achieved by using a 50 mW CW argon laser for 2 to 4 minutes. Based on the results of annealing behavior, this hole trap is believed to be due to vacancy related defect.

(2) For the LEC grown bulk GaAs, study of the effect of thermal annealing (200, 300, 500°C) in hydrogen ambient on the grown-in defects has been made. The results showed that for annealing temperatures below 300°C, there are four electron traps with energies of Ec-0.35, 0.46, 0.61 and 0.76 eV observed in all the samples studied, with trap density in the 10^{14} to 10^{15} cm^{-3} range. Thermal annealing reduces the density of these electron traps. However, for the 500°C annealed sample, a new electron trap with energy of Ec-0.83 eV (i.e., EL2) and density of 10^{15} cm^{-3} was observed in this sample, in addition to the E1 and E3 electron traps. The observation of EL2 level (As_{Ga} antisite defect) in GaAs annealed at 700 and 800°C has also been reported previously.

(3) For the MOCVD grown GaAs eppilayers on semi-insulating GaAs and Ge substrates, DLTS results showed that there is only one electron trap with energy of Ec-0.60 eV and density of 10^{16} cm^{-3} observed in the epilayer grown on S.I. GaAs substrate and one hole trap with energy of Ev+0.75 eV and density of 10^{13} cm^{-3} observed in epilayer grown S.I. Ge substrate. The drastic change in defect spectrum in these two samples is quite interesting, and further study is being undertaken to find out physical reasons for the change in defect spectrum observed in these samples.

(4) For the one-MeV electron irradiated LPE GaAs epilayers, a detailed study of deep-level electron and hole traps induced by the one-MeV electron irradiation under different electron fluxes, fluences, and annealing conditions has been carried out in this work. Defect parameters such as energy levels, defect density, capture cross section for each electron and hole trap have been determined from the DLTS data. Low temperature thermal annealing and recombination enhanced annealing studies have also been carried out in this work. Details of the results are described in this report.

TABLE OF CONTENTS

I. INTRODUCTION

III-V semiconductor materials formed from the elements Al, Ga and In in the Group III column and from the elements P, As and Sb in the Group V column are presently receiving intense investigation. The motivation for the research is found in two principal advantages offered by III-V compounds over silicon: The first advantage is the flexibility in the chioce of material systems such as the binary, ternary and quarternary compound semiconductors with a significant difference in physical, optical and electrical properties which could be used for a wide variety of device applications. A Group III atom will combine with a Group V atom to yield nearly stoichiometric binary semiconductor compound resulting in nine possible systems with different energy bandgaps and lattice constants; this is shown in Fig. 1.1. Each solid point in Fig. 1.1 represents the values for the particular compound listed. The continuous substitution of a cation for another cation or an anion for another anion is represented by a line in the figure. The substitution of both a cation and an anion leads to an enclosed area of permissible lattice parameters and corresponding bandgap energies. Thus, the entire area enclosed in Fig.1.1 is accessible to the device engineers when ternary and quarternary III-V solid solutions are employed. The solid line stands for a direct bandgap while the dashed line represents an indirect bandgap. The compounds with an asterisk are currently available in bulk single crystal form. The second advantage offered by the III-V materials is a general improvement in electrical properties. For examples,

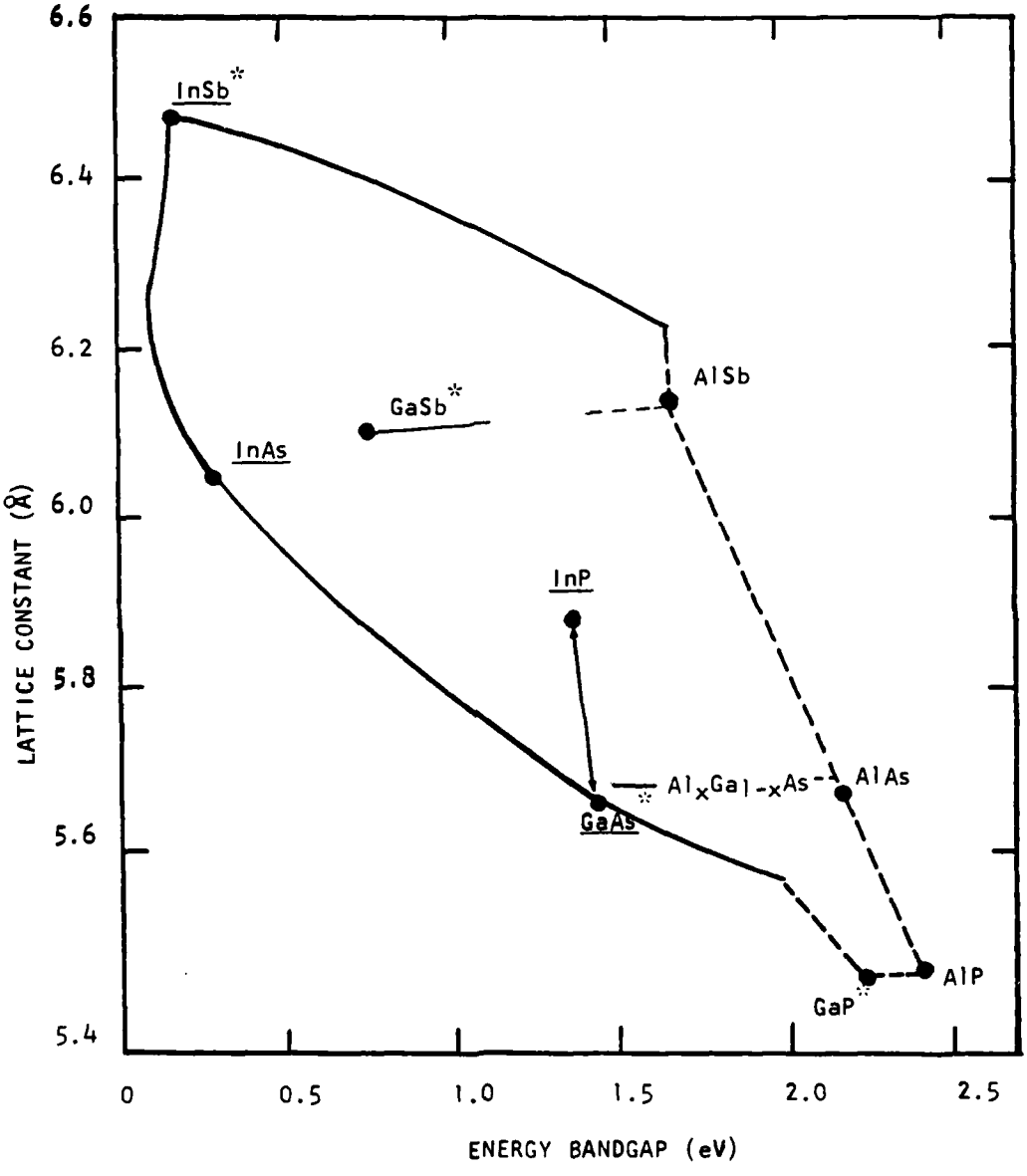

Fig.1.1 Lattice parameter vs energy bandgap for III-V compound semiconductors; —— direct gap, --- indirect gap; * available in bulk form.

the electron mobilities observed in III-V compounds can be as much as two orders of magnitude higher than silicon (e.g. un = 77,000 for InSb as compared to 1450 cm2/V.s for silicon); this is extremely important for the high speed or high frequency device applications. Thus, in the future, III-V compound semiconductors are expected to play an increasing important role as the host materials for semiconductor device applications.

In order to realize this progress, many technological problems as well as fundamental understanding of the material properties must be solved. Once the availability of device quality substrates is provided, attention should be focussed on the growth and characterization of epitaxial films--the home of the actual device. The epitaxial deposition of III-V thin films can be broadly classified according to the phase from which the solid film is deposited. Most of the III-V epitaxial films currently available are grown by the Liquid Phase Epitaxy (LPE), Vapor Phase Epitaxy (VPE), and the Organometallic Chemical Vapor Deposition (MOCVD) techniques. Molecular Beam Epitaxy (MBE) technique has also been widely used to grow III-V superlattice and multilayers structure.

Each of the epitaxy techniques cited above offers advantages and disadvantages, primarily as a result of different kinetic limitations. As is the case with silicon, the promising growth method from high quality and controllable, large scale production view is the chemical vapor deposition technique. In this technique the Group III elements are transported to the substrate location as group III chlorides or as organometallic species

while the Group V elements are transported as hydrides, natural elements or organometallics. As a result of a thermal gradient, a gas-solid reaction is promoted, depositing the desired solid compound or solution.

The goal of this research program is to perform a detailed analysis of the grown-in defects and transport properties of the III-V epitaxial films grown by the LPE, VPE, and MOCVD techniques under different growth and annealing conditions. Three main tasks were performed in this research program during the past twelve months: (1) Characterization of grown-in defects in Zn-doped InP grown by LEC technique, and study the effects of low temperature thermal and laser annealing on the density of grown-in defects, (2) Study the effect of thermal annealing in the hydrogen ambient on the grown-in defects in bulk GaAs grown by the LEC technique, and (3) a detailed study of the annealing behavior of the deep level defects induced by one-MeV electron irradiation in GaAs epitaxial films grown by infinite solution liquid phase epitaxial technique. Section II depicts the main research accomplishments derived from the current AFOSR research program. Section III presents the results of defect and transport studies in InP. Section IV discusses the defect characterization in the bulk GaAs under different annealing conditions. Studies of deep-level defects induced by one-MeV electron irradiation in GaAs epilayers as functions of electron flux, fluence, and annealing conditions are discussed in section V. The summary and conclusions are given in section VI. Section VII lists the publications supported by this grant. References are given in section VIII.

II. Research Accomplishments

This section summarizes our major technical findings derived from the research program supported by the current AFOSR grant No.AFOSR-81-0187A. Some of our findings were depicted in our 1982 AFOSR Annual Technical Report and seven publications listed in section VII of this report. Our research efforts for the past twelve months have led us to the following technical findings as a result of our collaboration with several governmental and industrial laboratories:

(1) Through the research collaboration with Dr. K. Vaidyanathan of Hughes Research Laboratory, the defect characterization in the LEC grown Zn-doped InP has been carried out by using the DLTS technique. In addition, the effects of thermal and laser annealing on the defect density in the LEC grown Zn-doped InP have also been studied. The results are presented in this report.

(2) Through the collaboration with Dr.P. W. Yu, work on the study of native defects in bulk GaAs grown by the LEC technique has resulted in the finding of an intrinsic double acceptor (i.e., Ev+0.077 eV hole trap). It is shown that p-type conduction is due to the presence of the shallow acceptor C(As) and the cation antisite double acceptor Ga/As. The first and second ionization energies determined for GaAs antisite are 77 and 230 meV from the valence band. Density of this defect was found in the low 1xE16 cm-3 range. It is noted that this intrinsic double acceptor may be responsible for the high resistivity (due to compensation) observed in the undoped GaAs substrate material. In addition,

study of the effect of the thermal annealing in the hydrogen environment on the deep-level defects in bulk GaAs samples have been carried out, and the results are discussed in section IV.

(3) Through the collaboration with Drs. R. Y. Loo and W. P. Rahilly, a detailed study of deep-level defects induced by one-MeV electron irradiation in n-type GaAs LPE layers fabricated by the infinite solution melt liquid phase epitaxial (LPE) technique has been carried out, and the results were presented at the 16th IEEE Photovoltaic Specialists Conference. Highlights of this study include: (a) a detailed characterization of both hole and electron traps induced by the one-MeV electron irradiation as functions of electron fluence and flux, (b) study of the effect of low temperature thermal annealing (Ta < 300°C) on the hole and electron traps; the results showed that certain shallow traps can be annealed out by this technique, while the density of deep-level traps can also be reduced drastically through low temperature and forward bias injection annealing processes. Additional studies are currently being undertaken to determine the annealing activation energy and defect annealing rate for each trap subject to different annealing conditions. Details of the results of our defect studies in the one-MeV electron irradiated GaAs LPE layers under different fluxes, fluences, and annealing conditions are discussed in section V of this report.

(4) Through collaboration with Dr. J. Parsons of Hughes Research Lab., a comparative study has been initiated on the deep-level defects in the MOCVD epitaxial films grown on the semi-insulating

GaAs and Ge substrates; the results obtained so far indicate that for Sn-doped GaAs epilayer grown on the S.I. GaAs substrate there exists a Ec-Ø.6 eV electron trap with density of 2xE15 cm-3 while for the undoped- GaAs grown on S.I. Ge only a small hole trap with energy of Ev + Ø.75 eV and density of around 1xE13 cm-3 was observed. Low temperature thermal annealing and laser annealing on the Ec-Ø.6 eV electron trap showed little or no effect in the defect density reduction, suggesting that this electron trap may be due to impurity related defect. Another interesting result obtained from this study is that the activation energy of the electron trap observed in this Sn-doped GaAs epilayer is smaller than that of the EL2 electron trap level commonly observed in the VPE GaAs epitaxial films (i.e. Ø.6 eV vs Ø.83 eV). One possible explanation for this is that the reduction in the activation energy of this electron trap may be due to the interaction of "tin" with the antisite defect As(Ga) (i.e., EL2 level) to form an antisite-donor complex defect level (i.e. Ec-Ø.6Ø eV). Further study of the effect of the shallow donor level on the EL2 activation energy and density in the MOCVD grown GaAs epitaxial films will be made in this research program during the next reporting period.

(5) Through the research collaboration with Dr. K. Vaidyanathan of Hughes Research Laboratories, study has been made on the characterrization of the intrinsic defects in Zn-doped InP grown by the Liquid Encapsulated Czochralski (i.e.LEC) technique. The Al, Ag and Au-InP Schottky diodes were fabricated for our DLTS

study. Barrier heights of 0.7 to 0.9 eV were obtained for these diodes. Our DLTS results showed that one hole trap with energy of Ev+0.52 eV and density of 1 to 2xE15 cm-3 was observed in these Zn-doped InP samples. A thermal annealing study was made at 170 C on these InP samples for up to 32 hours. The defect annealing rate was found to be 0.025/hour. Our electric field dependence of the emission rate measurement shows that this hole trap is a donor-like deep level defect (the hole emission rate was found to decrease with square root of the electric field). Another interesting study on these Zn-doped InP LEC samples is concerned with the laser annealing experiment. A 50 mW CW argon laser was employed to study the effect of laser annealing on the deep-level defects in these InP samples. Annealing times of 2 to 4 minutes were employed in this study. The results showed that a similar reduction in the density of this hole trap was observed in the laser annealed Zn-doped InP samples. It should be mentioned here that if the laser powers were increased to 200 mW (C.W.) or higher, then the laser annealing will introduce new hole traps into the annealed InP samples similar to those observed in the one-MeV electron irradiated InP reported by Levinson et al.

In short, our research efforts sponsored by the current AFOSR grant have indeed yielded significant technical findings which are of vital importance to the understanding of deep level defects in the III-V epitaxial materials as well as to the progress of the III-V epitaxial films growth technology. Details of our research accomplishments are depicted in this report.

III. Study of Defects and Transport Properties in InP

3.1 Overview

Indium phosphide (InP) and its alloys in the III-V compound semiconductors are excellent candidates for microwave, laser and optoelectronic devices. InP can be prepared by the VPE, LPE, MBE, LEC or MOCVD technique. The preference of one process over the other depends mainly on the ease of control of growth and the perfection of the grown crystal lattice with respect to the absence of defects and the smoothness of the surface morphology. For examples, if the Vapor Phase Epitaxy (VPE) is chosen to grow InP, tow reaction processes can be used. These are the halide and the hydride processes. In the halide process, the reactants such as In, PCl3, and H2 are used, while for the hydride process the source reactants are In, HCl, PH3, and H2. Clarke et al used the halide process, and obtained a high carrier density around 1xE16 to 1xE17 cm-3 and low mobility. They attributed this to the formation of a phosphorus vacancy which contributed to the ionized impurity scattering. Wessel et al showed that in the hydride process, the growth kinetics are surface controlled rather than mass controlled. They observed that by increasing the PCl3 concentration or the HCl concentration would cause a decrease of the net donor density or the free carrier concentration in the InP. It was proposed that increase in HCl concentration will increase the partial pressure of HCl, which in turn reduces the silicon donor concentration and consequently

decreases the phosphorus vacancy density as shown by the reactio equation:

$$HX2 + V(p) \text{ ------> } X(p) + e + H2 \qquad (3.1)$$

where, V(p) is a phosphorus vacancy, H X2 is group III hydride.

Study of deep-level defects in the intrinsic or extrinsic InP as a result of the stoichiometry, kinetics and growth processes constitutes a significant research topic in recent years. Studies of grown-in defects in the undoped and doped InP grown by the VPE, LPE, MBE, and MOCVD techniques have been reported by various researchers, using DLTS, photocapacitance, as well as the photoluminescence techniques. Table 3. 1 summarizes the defect energy levels and possible physical origins of the defects for the n-type InP reported in the literature. The letter, V, stands for the vacancy defect and subscript, i, denotes the interstitial defect. For examples, V(In), represents an indium vacancy, P(i), denotes a phosphorus interstitial, and In(p) stands for a phosphorus in the In sublattice or simply called the antisite defect. A combination of all these point defects may create different types of defects such as divancy, di-interstitial, vacancy-impurity complex and others. Table 3.2 shows the native as well as radiation induced defects in the p-type indium phosphide crystal grown by various growth processes. It should be mentioned here that the defect information obtained so far for InP is quite scattered and far from conclusion. In particular, the physical origins of the reported deep-level defects are mostly unknown, and require further study.

Table 3.2 Deep-level Defects in p-Type InP

Trap levels Ev + ET (eV)	Growth process	Defect origin	Reference
0.50, 0.41 0.22, 0.09	VPE	Residual impurity	13
0.15	Mg-doped, LEC Zn-doped, LEC	Neutral trap	14 16
0.54, 0.37 0.33, 0.17	LPE, one-MeV electron irrad.	-	15
0.50, 0.34	one-MeV electron irradiation, Zn-doped, LEC	-	16

In this section, the results of our DLTS study on the native defects in Zn-doped InP grown by the LEC technique are presented. In addition, the effects of thermal and laser annealing on the grown-in defects in the Zn-doped InP are analyzed. Finally, the results of the resistivity and the Hall effect measurements on two n-type InP specimen are also included.

3.2 Defect characterization in LEC Grown Zn-doped InP

In order to perform the DLTS measurement on the Zn-doped InP, Schottky barrier diodes were fabricated on the Zn-doped InP specimen using Au, Ag, and Al metals. Fig. 3.1 shows the I-V characteristics curves for a Al-InP Schottky diode measured at different temperatures. The barrier height deduced from this plot is 0.78 eV. For the Ag-InP and Au-InP Schottky diodes, the barrier height was also found around 0.8 eV to 0.85 eV. Fig.3.2 shows the forward I-V characteristics curves for the Al-InP, Au-InP, and Ag-InP Schottky diodes. The diode ideality factor for these diodes varies between 1.23 to 1.46. The background carrier concentration in these LEC grown InP samples was determined by the C-V measurements with value around 1.5xE16 cm-3. The DLTS measurement was performed on these smaples to determine the density and the energy level of the native hole traps, and the results are discussed next.

Fig.3.3 shows the spatial dependence of the Ev+0.52 eV hole trap density as well as the background dopant density for the LEC grown Zn-doped InP sample. The result shows that this hole trap is uniformly distributed across the sample as is clearly shown in

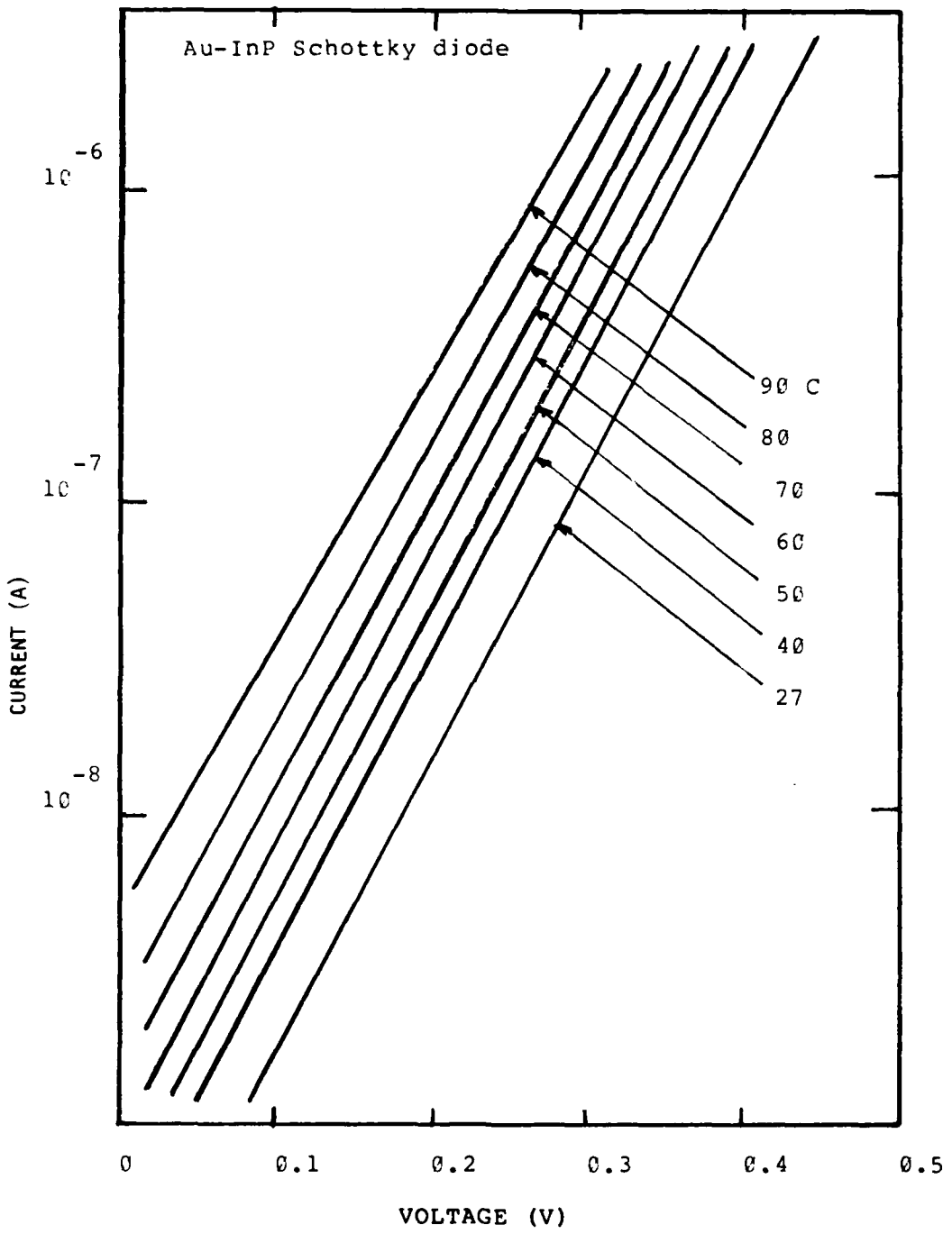

Fig.3.1 Forward I-V characteristics for Au-p-type InP Schottky diode as a function of temperature.

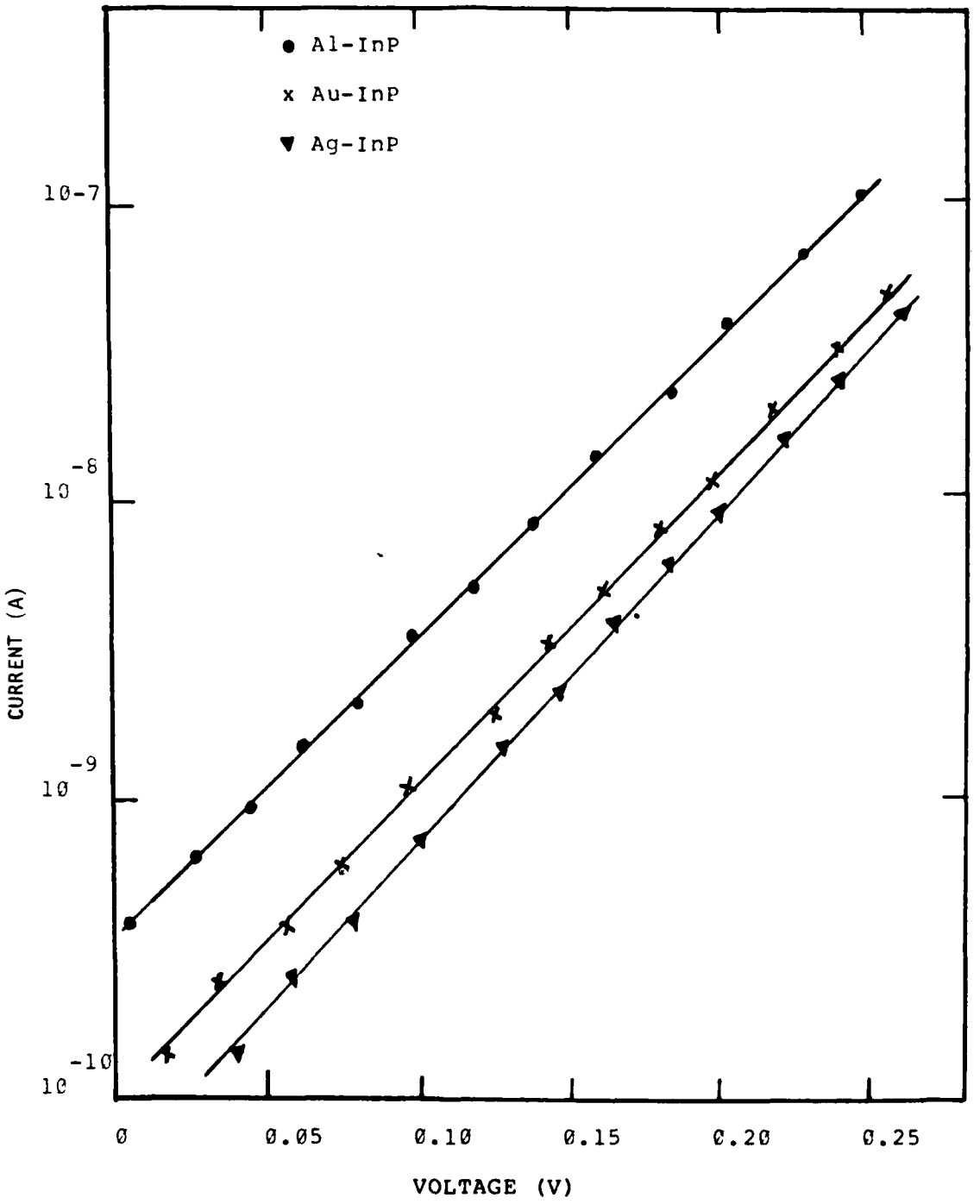

Fig.3.2 The forward I-V characteristics for the Al-, Au-, and Ag- p-type InP Schottky barrier diodes, at 300 K.

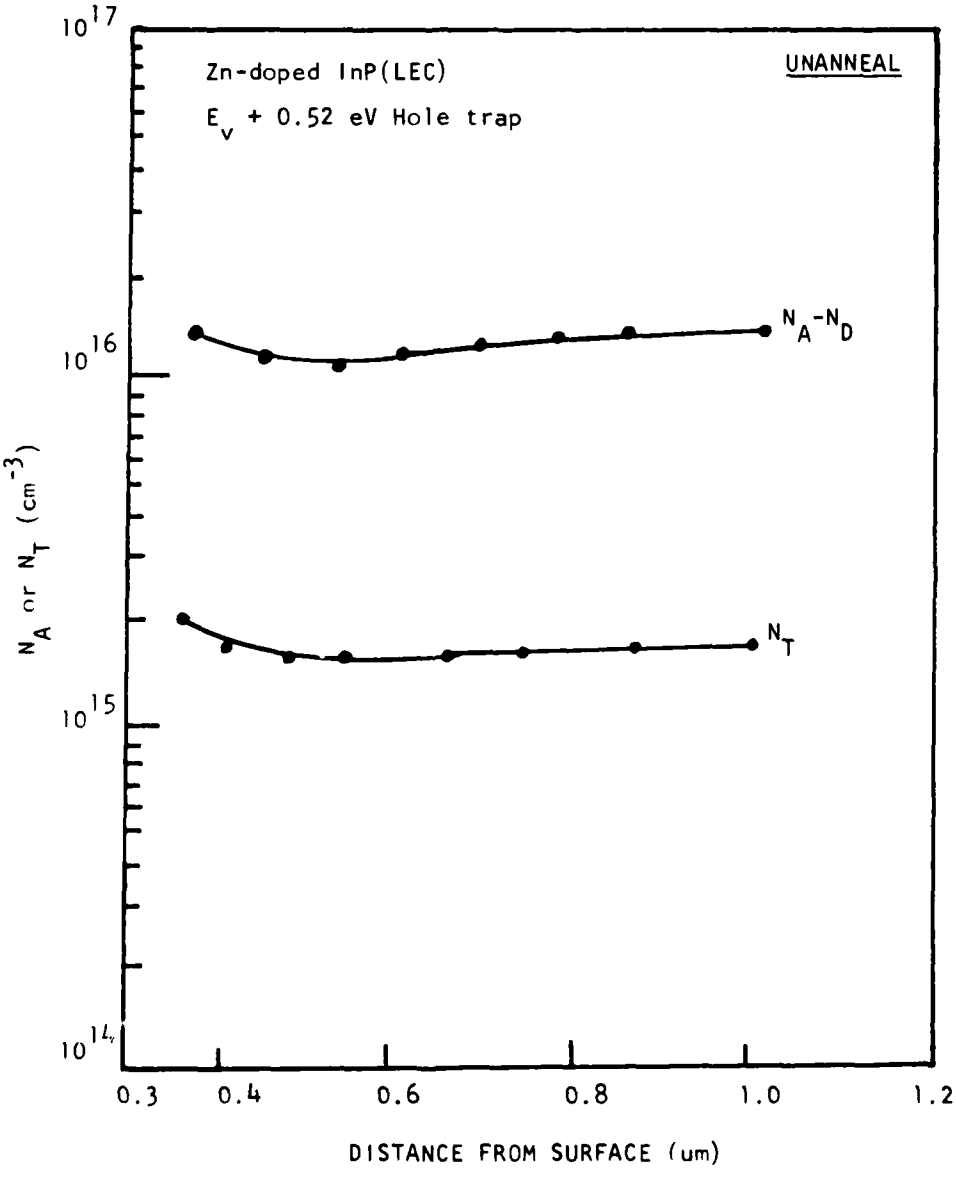

Fig.3.3 Spatial dependence of dopant density and trap density in Zn-doped InP grown by LEC technique.

Fig.3.3. Fig.3.4 shows the electric field dependence of the emission rate for this hole trap, which shows that the hole emission rate is directly proportional to the square root of the electric field; decreasing with increasing field strength. This result indicates that the observed hole trap is a donor type deep level defect, possibly due to the phosphorus vacancy related defect. The Arrhenius plot of hole emission rate, ep/T^2 vs 1/kT, for the hole trap is shown in Fig. 3.5. From the slope of this plot yields the activation energy of the hole trap, which is 0.52 eV. A comparison of this hole trap with those listed in Table 3.2, shows that a similar hole trap has also been observed in the one-MeV electron irradiated InP.

3.3 Effects of thermal and laser anneling on the grown-in defects in Zn-doped InP

To study the nature and the physical origin of the Ev + 0.52 eV hole trap, the effects of low temperature thermal annealing and laser annealing on the density of this hole trap were performed on the Zn-doped InP samples discussed above. The samples were thermally annealed at 170 C for 2, 4, 8, 16, and 32 hours, respectively. The laser annealing was also performed on the Zn-doped InP samples at 50 mW for 2 and 4 minutes, respectively. The results are displayed in Fig. 3.6 and Fig.3.7, respectively. From the DLTS data shown in Fig .3.6, the defect annealing rate for the hole trap in these Zn-doped InP samples was found to be 0.025 / hour; this is shown in Fig.3.8. From the results of thermal and laser annealing study of this hole trap as well as Fig.3.3, it is obvious that the Ev + 0.52 eV hole trap

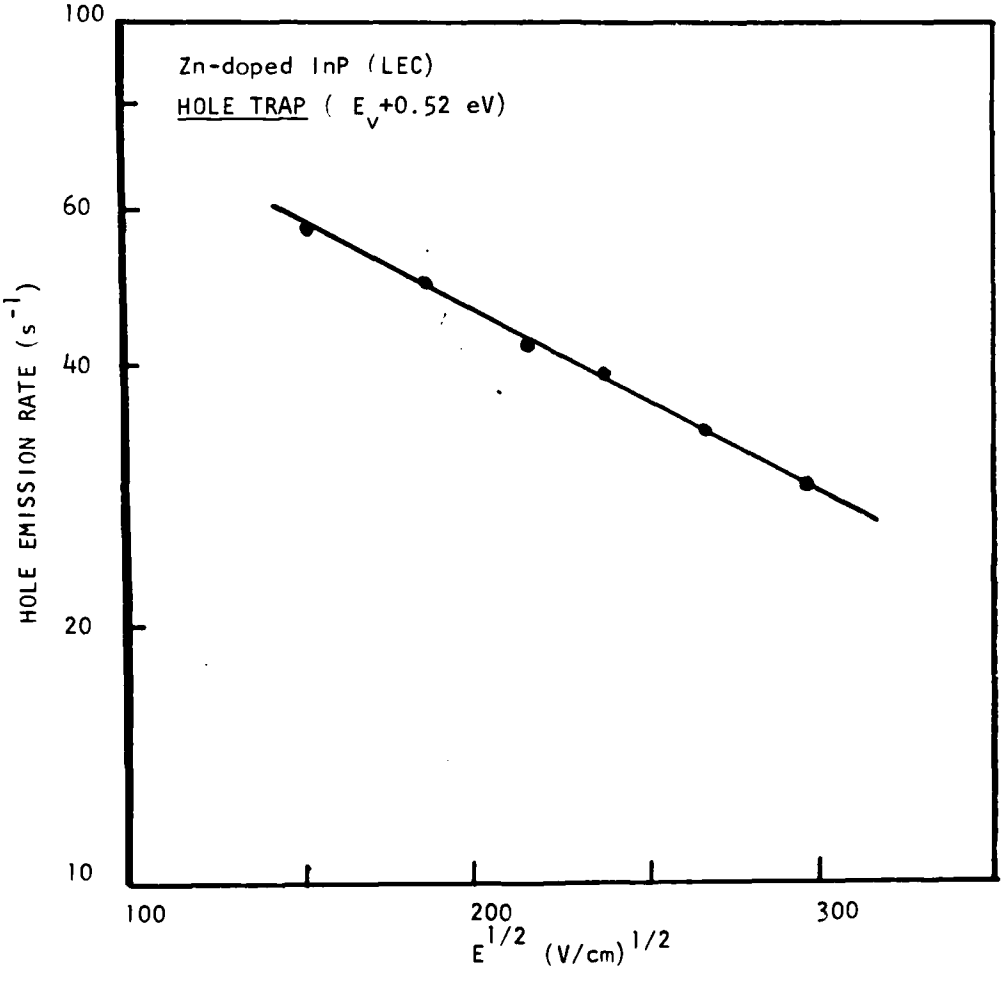

Fig.3.4 Hole emission rate vs square root of electric field for Zn-doped InP grown by LEC technique.

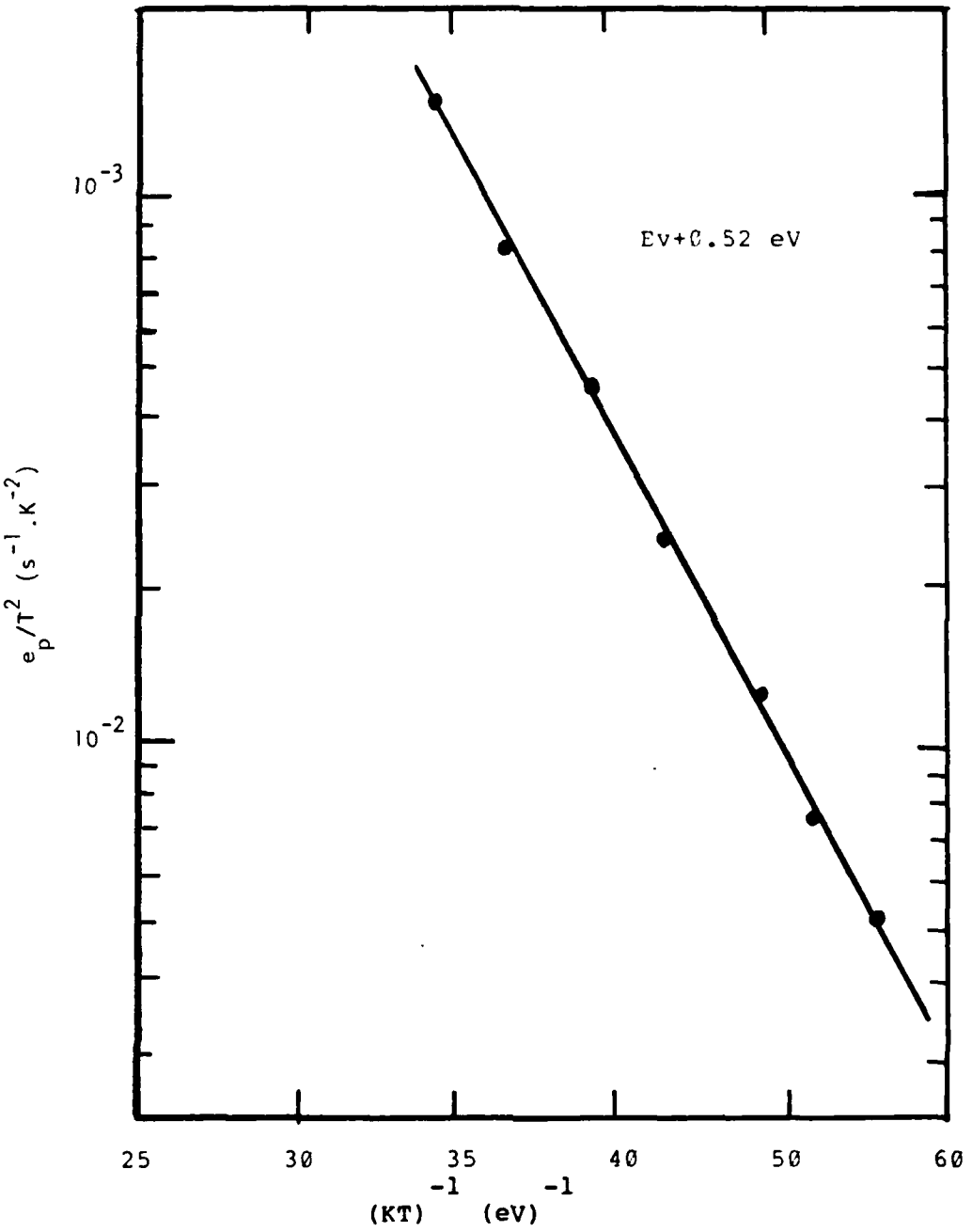

Fig. 3.5 Hole emission rate vs inverse temperature for Zn-doped InP.

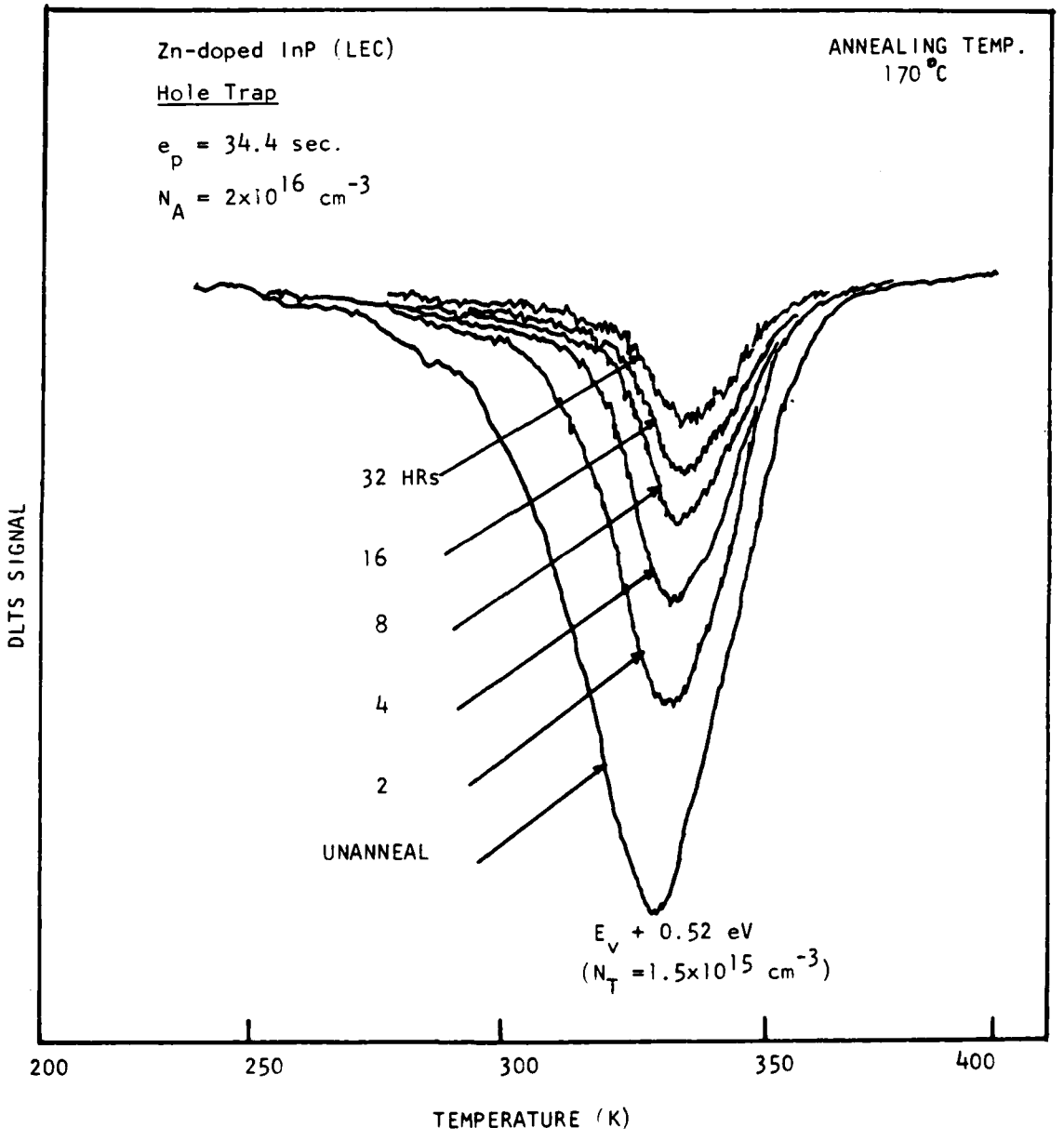

Fig.3.6 DLTS scans of hole trap in Zn-doped InP grown by LEC technique as a function of thermal annealing time. T_A = 170 °C

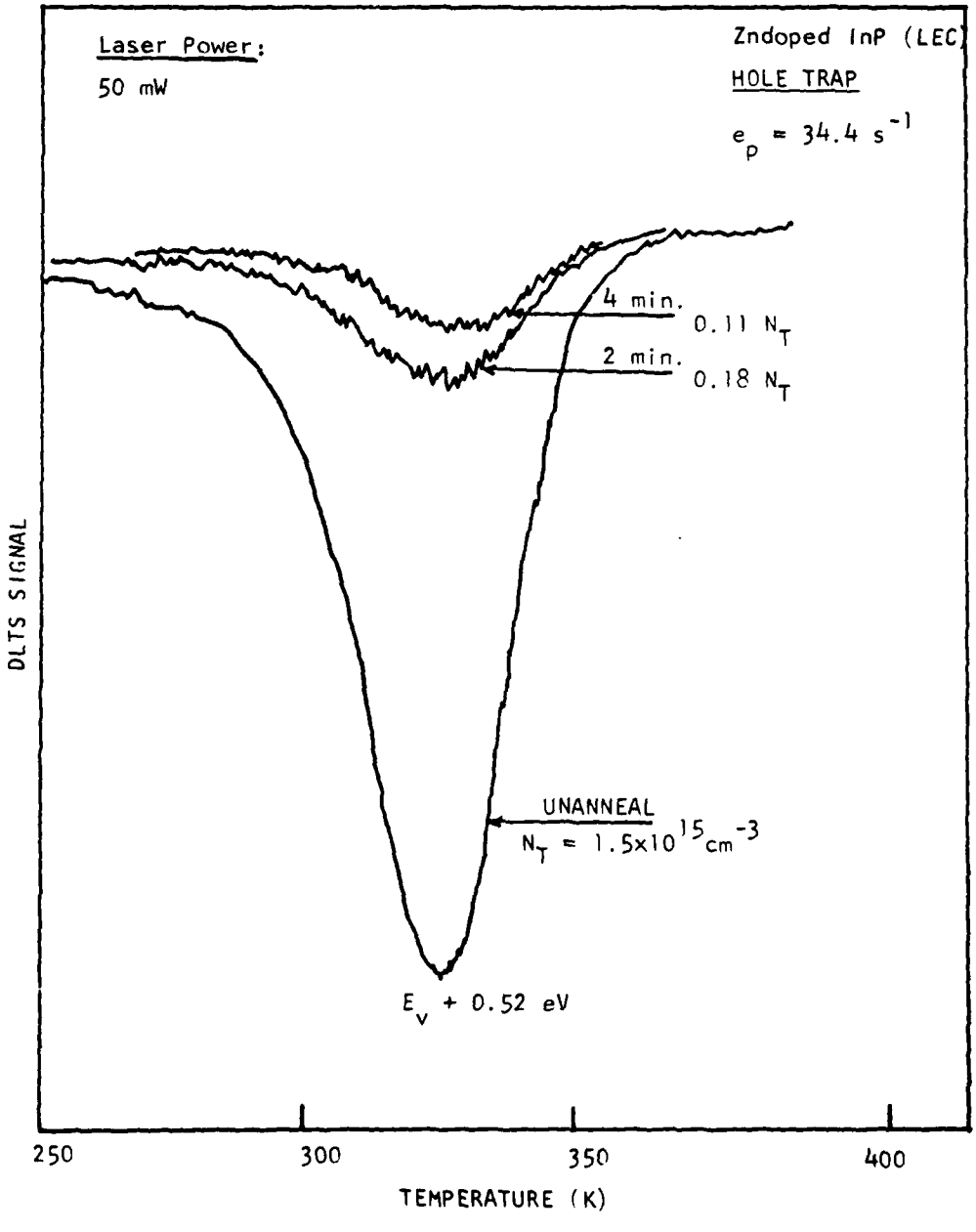

Fig. 3.7 DLTS scans of hole trap vs laser annealing time for Zn-doped InP grown by LEC technique.

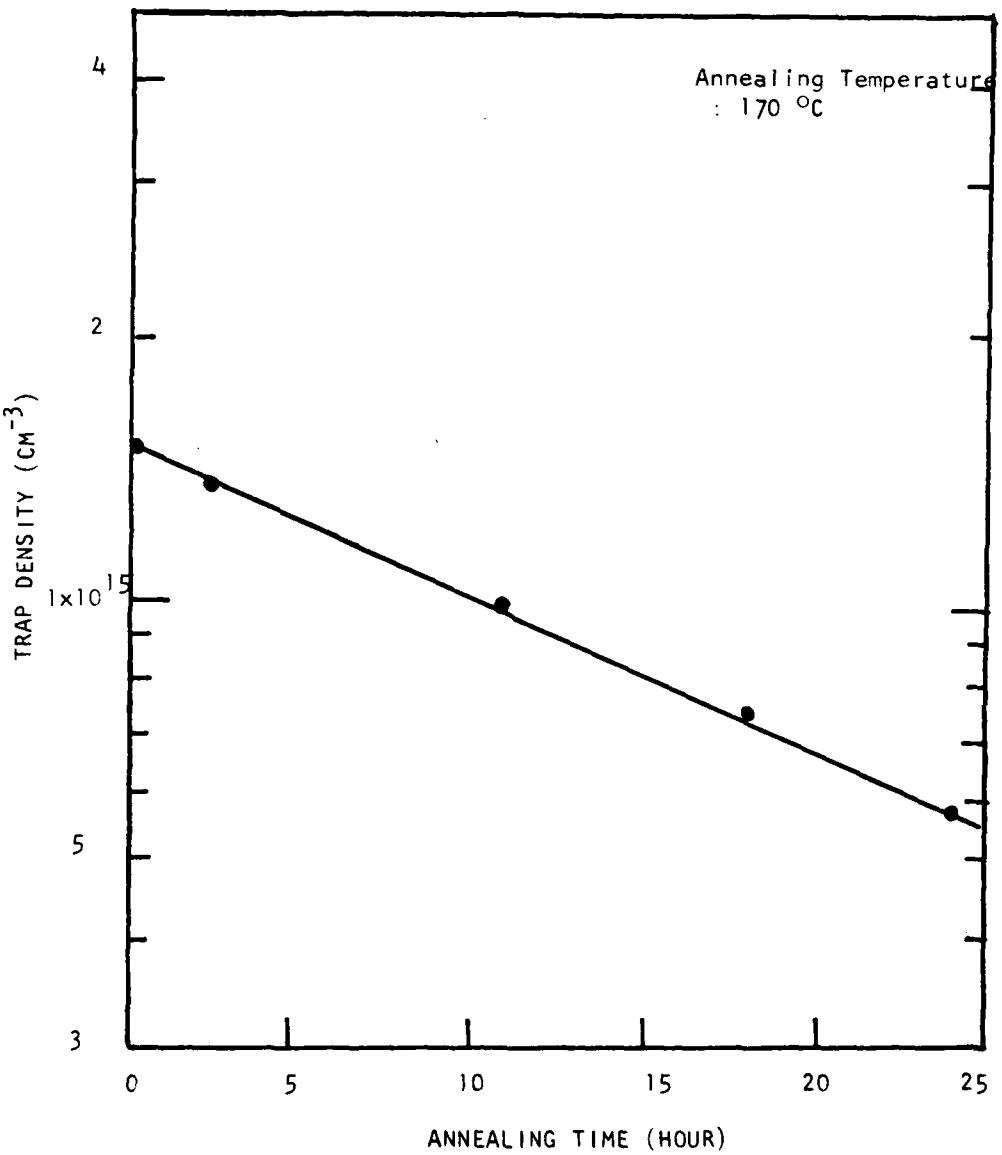

Fig. 3. 8 Density of hole trap vs annealing time for Zn-doped InP.

is not impurity related defect. Based on the fact that this hole trap is quite sensitive to the annealing conditions, and that it has been observed in the one-MeV electron irradiated InP, the most likely origin of this hole trap is due to phosphorus vacancy related defect rather than the residual impurities. In order to find out physical origin of this hole trap, new samples of InP are currently being prepared for additional DLTS study of both the electron and hole traps in the InP grown by different growth techniques and different heat treatment.

3.4 Transport Measurements in n-Type InP

In order to study the transport properties in InP, several bulk n-type InP samples have been prepared for the resistivity and Hall effect measurements, using the square Van der Pauw test structure. The results of the resistivity and Hall effect measurements are shown in Fig. 3.9, Fig.3.10, and Fig.3.11, respectively. Both the temperature dependence of carrier density and Hall mobility in these n-type InP bulk samples were deduced from these measurements for temperatures between 77 and 300 K. It is noted that the electron concentration in these samples is quite high (around 1xE17 cm-3), and the maximum electron mobility is around 4000 cm2/V.s at 150 K. For temperature below 150 K, the impurity scattering becomes dominant, while the acoustic phonon scattering takes over for temperature above 150 K. This result was found in good agreement with those reported in the literature for the InP materials. We plan to perform more transport measurements on the InP epitaxial layers to be grown by the MOCVD and MBE techniques under different growth conditions.

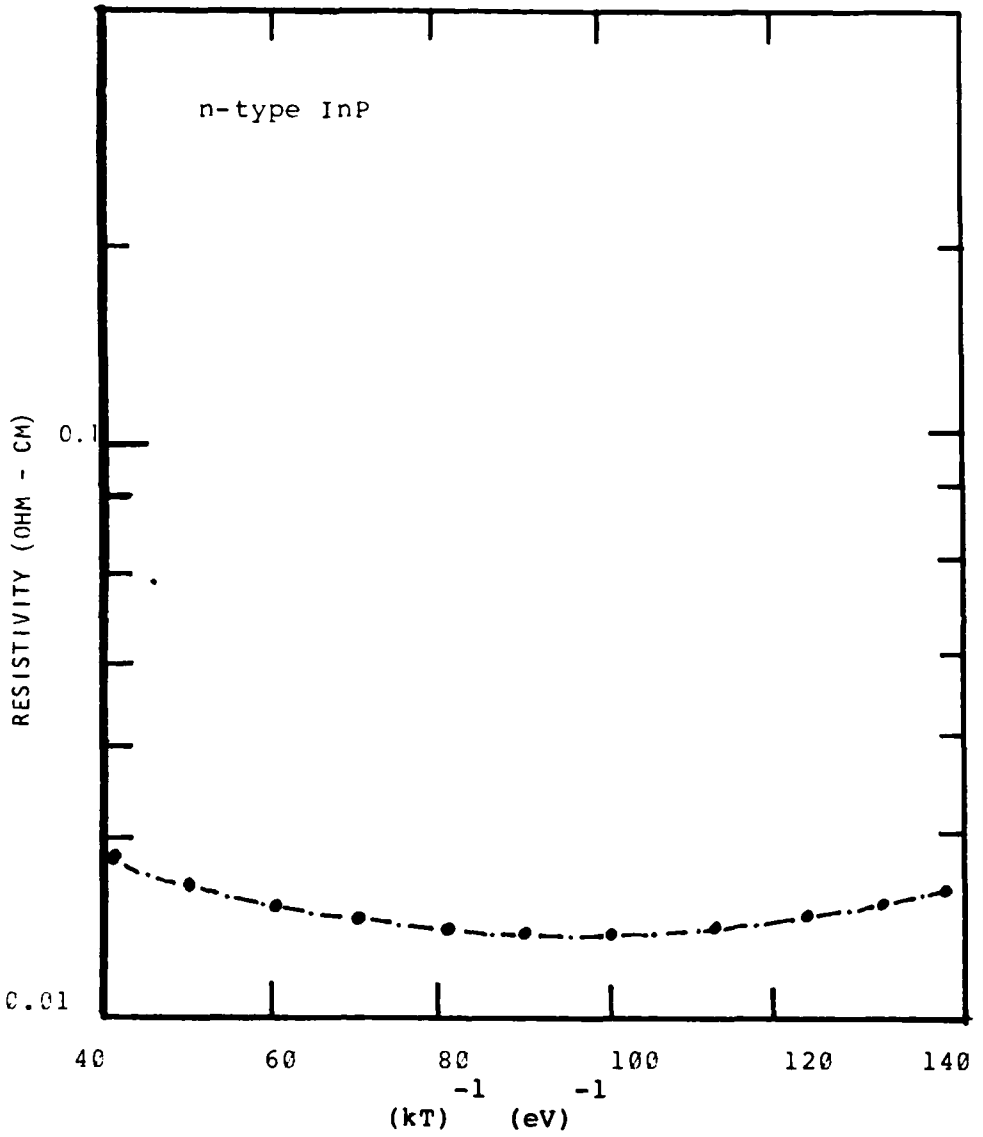

Fig. 3.9 Resistivity vs inverse temperature for n-type InP.

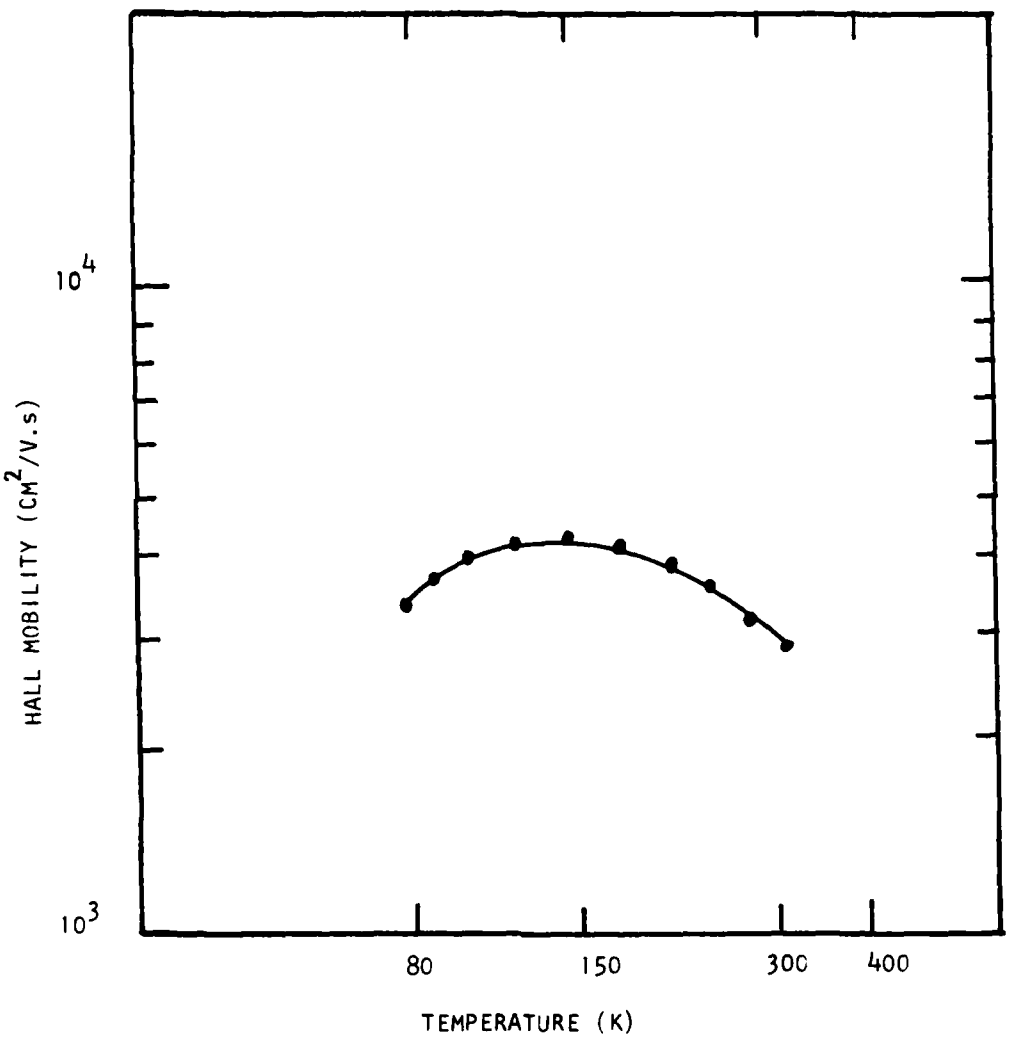

Fig. 3.10 Hall mobility vs temperature for n-type InP.

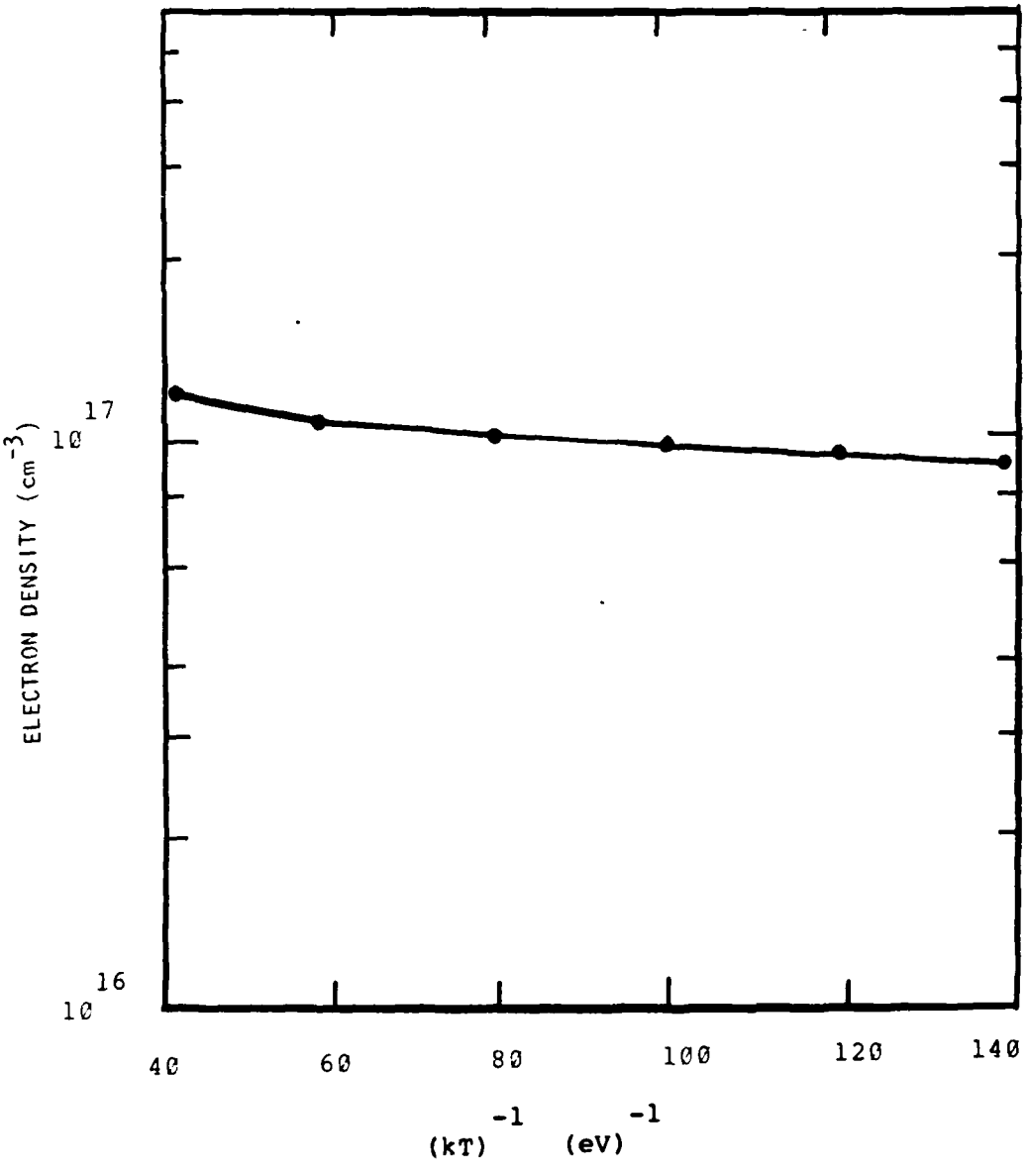

Fig. 3.11 Electron density vs inverse temperature for n-type InP.

IV. Defect Characterization in n-GaAs Grown by the LEC and the MOCVD Techniques

4.1 Overview

To study the native defects in a semiconductor material it is important to get familiar with certain aspects of the crystal growth. For examples, the bulk GaAs single crystal can be grown by the Bridgeman-Stockbarger and the Czochralski pulling methods. Fig.4.1 shows the phase diagram of the GaAs in various states. It is well known that the bulk GaAs is usually grown at high temperatures (i.e., T > 800 C), while the epitaxial growth is normally carried out at lower tempratures (i.e.,between 700 and 800 C). As a result, the defect density in the bulk GaAs is expected to be higher than the epitaxially grown GaAs. This can be best explained via the phase diagram shown in Fig.4.1 for GaAs. Bulk GaAs crystal is usually grown at 1100 C or higher; in this case the wider solubility curve (dash line in the center curve) indicates that the crystal will have higher derivative percentage of As atoms. In Ga-rich condition, lower arsenic atomic percentage will produce higher gallium vacancy, higher arsenic interstitial, or higher As(Ga) antisite defects. In As-rich condition, higher arsenic atomic percentage will produce higher arsenic vacancy, higher gallium interstitial or higher Ga(As) antisite. On the other hand, epitaxial growth of III-V compound semiconductors is usually carried out between 600 and 800 C, and thus the lower defect density and purer epilayer are expected than that of the bulk grown material.

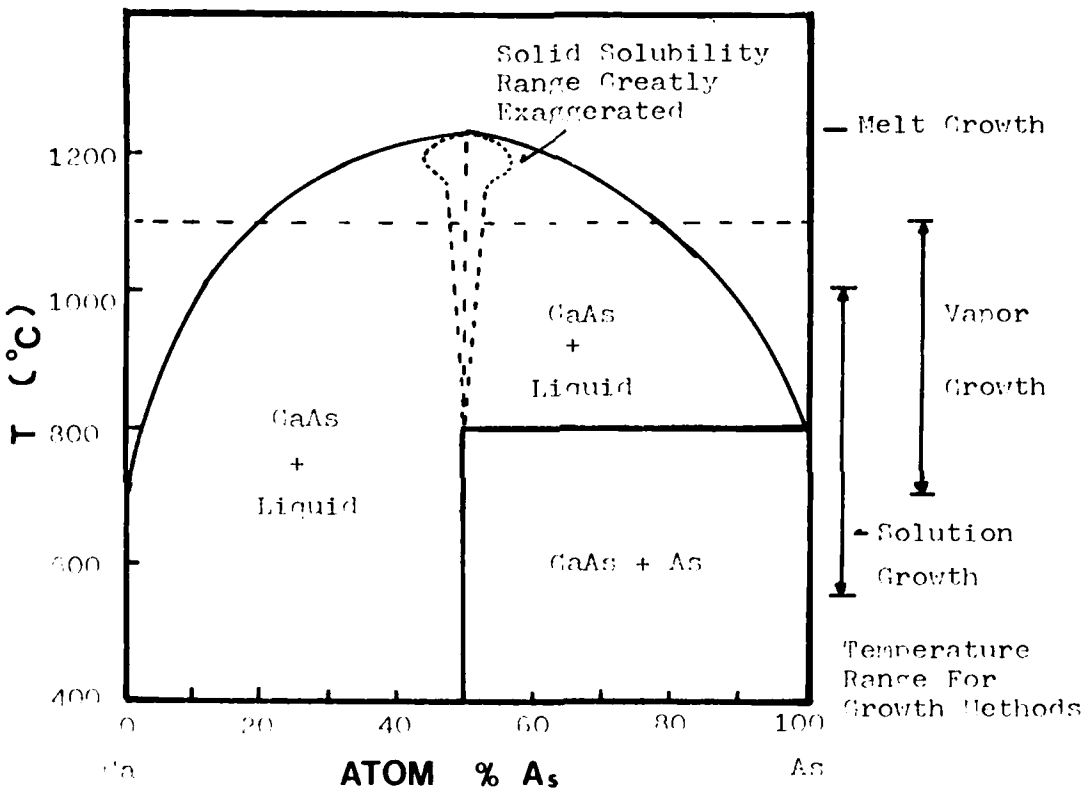

Fig. 4. 1 The phase diagram for GaAs.

Table 4.1 Electron traps in n-type GaAs

Level	Activation energy (eV)	Capture cross section (cm2)	Growth method	Reference
ET1	Ec-0.85	6.5xE-13	Bulk	27
ET2	0.30	2.5xE-15	"	
ES1	0.83	1.0xE-13	Bulk	28
EF1	0.72	7.7xE-15	Cr-doped bulk	29
EI1	0.43	7.3xE-16	VPE	55
EI2	0.19	1.1xE-14	VPE	
EI3	0.18	2.2xE-14	VPE	
EB1	0.86	3.5xE-14	Cr-doped LPE	30
EB2	0.83	2.2XE-13	As-grown VPE	30
EB3	0.90	3.0xE-11	Elec. Irrad.	31
EB4	0.71	8.3xE-13	" "	
EB5	0.48	2.6xE-13	MBE	56
EB6	0.41	2.6xE-13	Elec. Irrad.	31
EB7	0.30	1.7xE-14	MBE	56
EB8	0.19	1.5xE-14	MBE	56
EB9	0.18	-	Elec. irrad.	31
EB10	0.12	-	" "	31
EL1	0.78	1.0xE-14	Cr-doped bulk	57
EL2 (A)	0.83	1.2xE-13	VPE	
EL3 (B)	0.58	"	"	"
EL4	0.51	1.0xE-12	MBE	
EL5 (C)	0.42	1.2xE-13	VPE	
EL6	0.35	1.5xE-13	Bulk	"
EL7	0.30	7.2xE-15	MBE	
EL8 (D)	0.28	7.7xE-15	VPE	
EL9	0.23	6.8xE-15	"	32
EL10	0.17	1.8xE-15	MBE	
EL11 (F)	0.17	3.0xE-16	VPE	
EL12 (A)	0.78	4.9xE-12	"	"
EL14	0.22	5.2xE-16	Bulk	
EL15	0.15	5.7xE-13	Elec. irrad.	31
EL16	0.37	4.0xE-18	VPE	

Table 4.2 Hole Traps in p-type GaAs

Level	Activation energy (eV)	Capture cross section (cm2)	Growth method	Reference
HT1	Ev+0.44	1.2xE-14	VPE	27
HS1	0.58	2.0xE-19	LPE	28
HS2	0.64	4.1xE-16	"	28
HS3	0.44	4.8xE-18	"	28
HB1	0.78	5.2xE-16	Cr-doped LPE	30
HB2 (B)	0.71	1.2xE-14	As-grown LPE	"
HB3	0.52	3.4xE-16	Fe-doped LPE	"
HB4	0.44	3.4xE-14	Cu-doped LPE	"
HB5 (A)	0.40	2.2xE-13	As-grown LPE	"
HB6	0.29	2.0xE-14	Elec.Irrad.	31
HL1	0.94	3.7xE-14	Cr-doped VPE	32
HL2	0.73	1.9xE-14	As-grown LPE	32
HL3	0.59	3.0xE-15	Fe-doped VPE	33
HL4	0.42	"	Cu-doped VPE	34
HL5	0.41	9.0xE-14	As-grown LPE	33
HL6	0.32	5.6xE-14	VPE	34
HL7	0.35	6.4xE-15	MBE	34
HL8	0.52	3.5xE-16	MBE	"
HL9	0.69	1.1xE-13	VPE	"
HL10	0.83	1.7xE-13	VPE	"

From the mass action law, Eq.(4.1) through (4.5) can be expressed by:

$$K1 = [As(i)]\,[V(As)] = 2.92xE6\ \exp(-4.845/kT) \quad (4.6)$$

$$K2 = [As^{+}]\,n/[V(As)] = 442\ \exp(-0.27/kT) \quad (4.7)$$

$$K3 = [As(i)^{+}]\,n/[As(i)] = 4.9xE\text{-}9\ T\hat{}3/2\ \exp(-0.4/kT) \quad (4.8)$$

$$K4 = np = 1xE\text{-}12\ T\hat{}3\ \exp(-1.62/kT) \quad (4.9)$$

$$K5 = [As(i)]\ /\ P(As)2\hat{}1/2 = 16.4\ \exp(-1.125/kT) \quad (4.10)$$

, and the charge neutrality condition can be written as

$$n = p + [V(As)^{+}] + [As(i)^{+}] \quad (4.11)$$

There are six unknown in Eqs.(4.6) to (4.11), and we can solve these six unknowns in term of the arsenic partial pressure P(As)2 and temperature. Fig. 4.2 shows the defect concentrations as a function of the P(As)2 for T = 700 C.

For the extrinsic GaAs, we need to consider the formation of a gallium Frenkel defect and the impurity complex. The gallium Frenkel defect is given by

$$Ga(Ga) + V(i) = Ga(i) + V(Ga) \quad (4.12)$$

The numbers of defect on the two sublattices are coupled through the Schottky reaction

$$0 = V(Ga) + V(As) \quad (4.13)$$

The ionization reaction is given by

$$V(Ga) = V(Ga)^{-} + h^{+} \quad (4.14)$$

, and the formation of the interstitial pairs is

$$Ga(i) + As(i) = Ga(i)As(i) \quad (4.15)$$

Now consider a Te-doped GaAs. If a tellurium atom is replaced by a As atom from the host lattice site, then the reaction equation

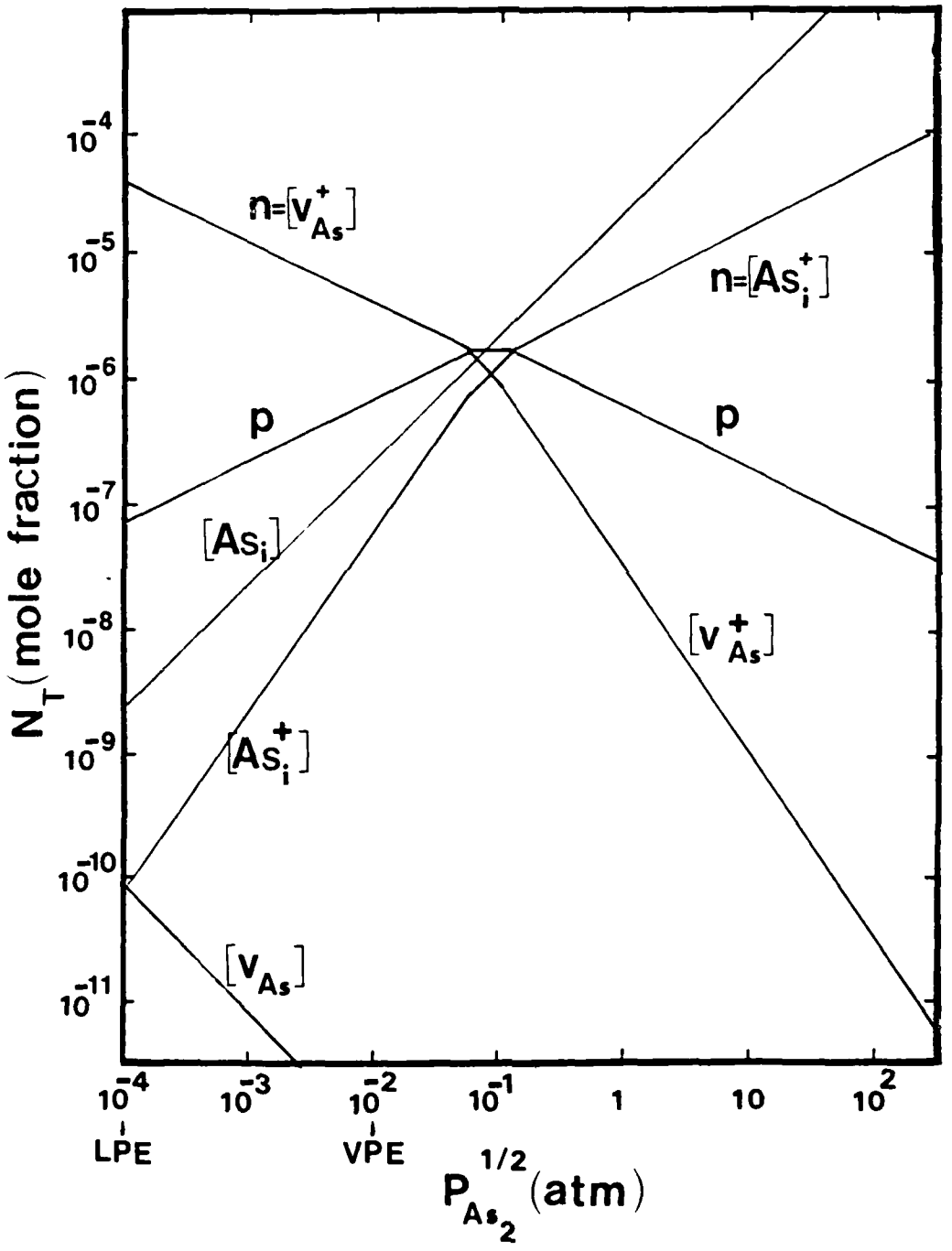

Fig. 4.2 Defect density vs arsenic partial pressure for GaAs at growth temperature of 700 °C.

can be written as

$$Te(i) + V(As) = Te(As)^{+} + e^{-} \qquad (4.16)$$

, and the reaction equation for the impurity complex is given by

$$Te(As)^{+} + V(Ga)^{-} + Te(As)V(Ga)^{-} + h^{+} \qquad (4.17)$$

Charge neutrality equation for the Te-doped GaAs is

$$n + V(Ga)^{-} + Te(As)V(Ga)^{-} = p+V(As)^{+} + As(i)^{+} + Te(As)^{+} \qquad (4.18)$$

The defect concentrations for the $V(As)^{+}$, $As(i)^{+}$, $Te(As)^{+}$, $Te(As)^{+}$, $Te(As)V(Ga)^{-}$, $V(Ga)^{-}$ can be calculated from Eqs.(4.6) to (4.10) and (4.12) to (4.18).

4.2 Effect of Hydrogen Annealing on the Grown-in Defects in the LEC Grown GaAs

In this section, we present the results of our study of the native defects observed in the LEC grown bulk GaAs. Study the effect of heat treatment on the native defects performed on these samples at 200, 300, and 500 C for one hour in H2 ambient has also been carried out in this work.

In the following, the results of the thermally-stimulated-capacitance (TSCAP) and the Deep-Level-Transient-Spectroscopy (DLTS) measurements on the LEC grown GaAs samples are discussed.

Native defects in the LEC grown GaAs were characterized by the TSCAP and the DLTS methods as a function of the annealing temperature. Defect density and energy levels as well as the spatial dependence of the defect density were determined from these measurements.

Fig. 4.3 shows the TSCAP scans in the LEC grown GaAs Schottky diodes taken at a reverse bias of -2 Volts. From this figure, it is noted that the capacitance values for samples annealed at 200 and 300 C for one hour in H2 ambient show little change from the unannealed sample. However, as the annealing temperature raises to 500 C, the capacitance value decreases by more than fifty percent from the unannealed sample, indicating a large reduction in free carrier density in the 500 C annealed sample. This may be due to the introduction of the EL-2 electron trap (i.e., Ec - 0.83 eV) by the 500 C annealing process, as is evidenced by our DLTS data. The capacitance steps observed in the TSCAP scans such as those occurred at 130 and 240 K for sample annealed at 500 C are due to the electron emission from the corresponding electron traps; the exact energy level for these electron traps, however, can be determined more readily by using the DLTS technique to be discussed next.

The DLTS scans of electron traps (i.e., majority carrier traps) for the LEC grown GaAs annealed at 200, 300, and 500 C for one hour in H2 ambient are shown in Fig. 4.4 through Fig 4.7, and the defect parameters deduced from the DLTS measurements are summarized in Table 4.3. For samples unannealed or annealed at 200 and 300 C for one hour, there are four electron traps with energies of E1 = Ec - 0.35, E2 = Ec- 0.46, E3 = Ec - 0.61, and E4 E4 = Ec - 0.76 eV observed in these samples. As the annealing temperature increases to 500 C, a new electron trap level with energy of Ec - 0.83 eV (i.e. EL2-level) is emerged into the DLTS spectrum along with two other electron traps (i.e.,E1 and E3),

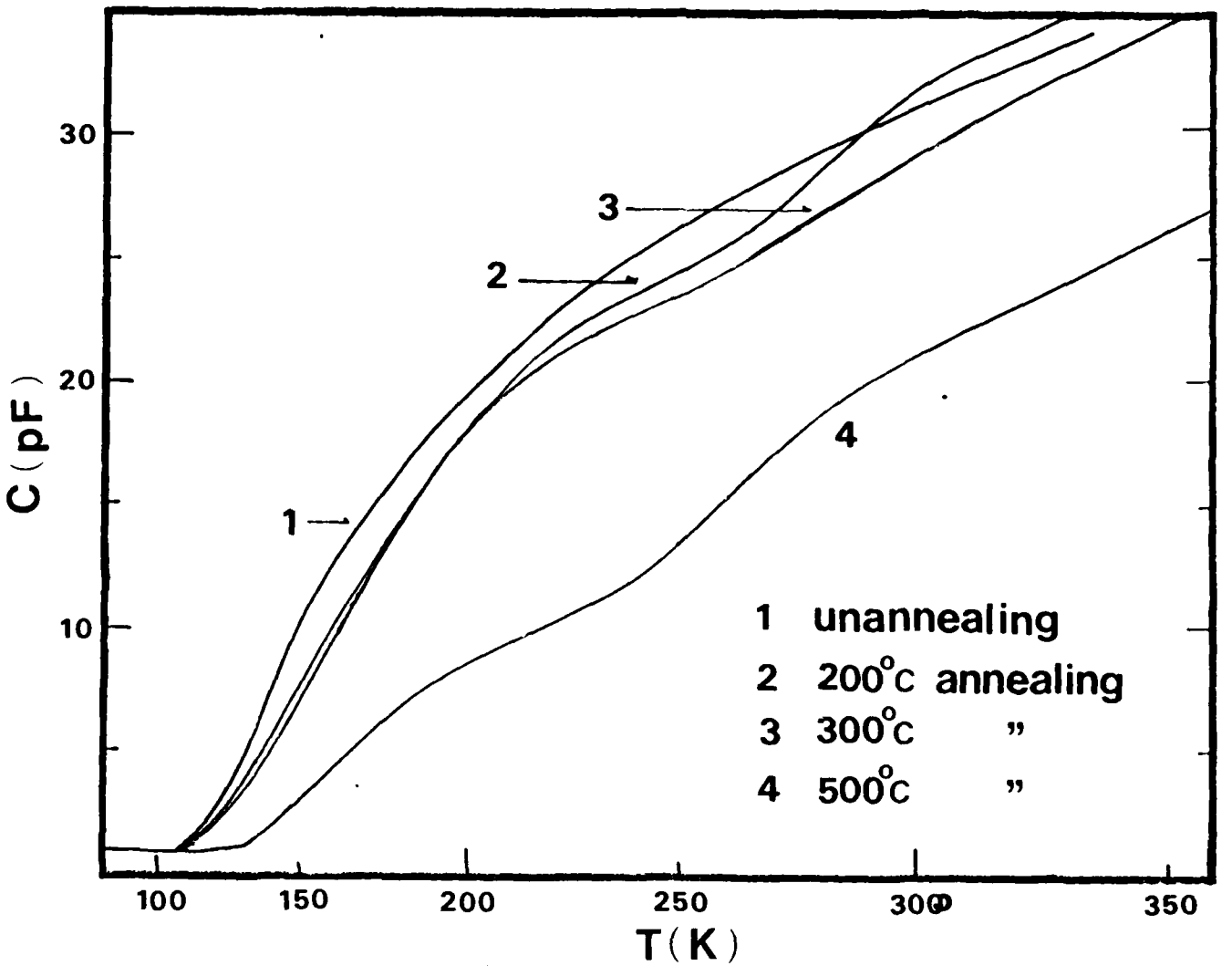

Fig. 4.3 Thermally Stimulated Capacitance (TSCAP) measurements for the as-grown and thermally annealed GaAs samples grown by LEC technique.

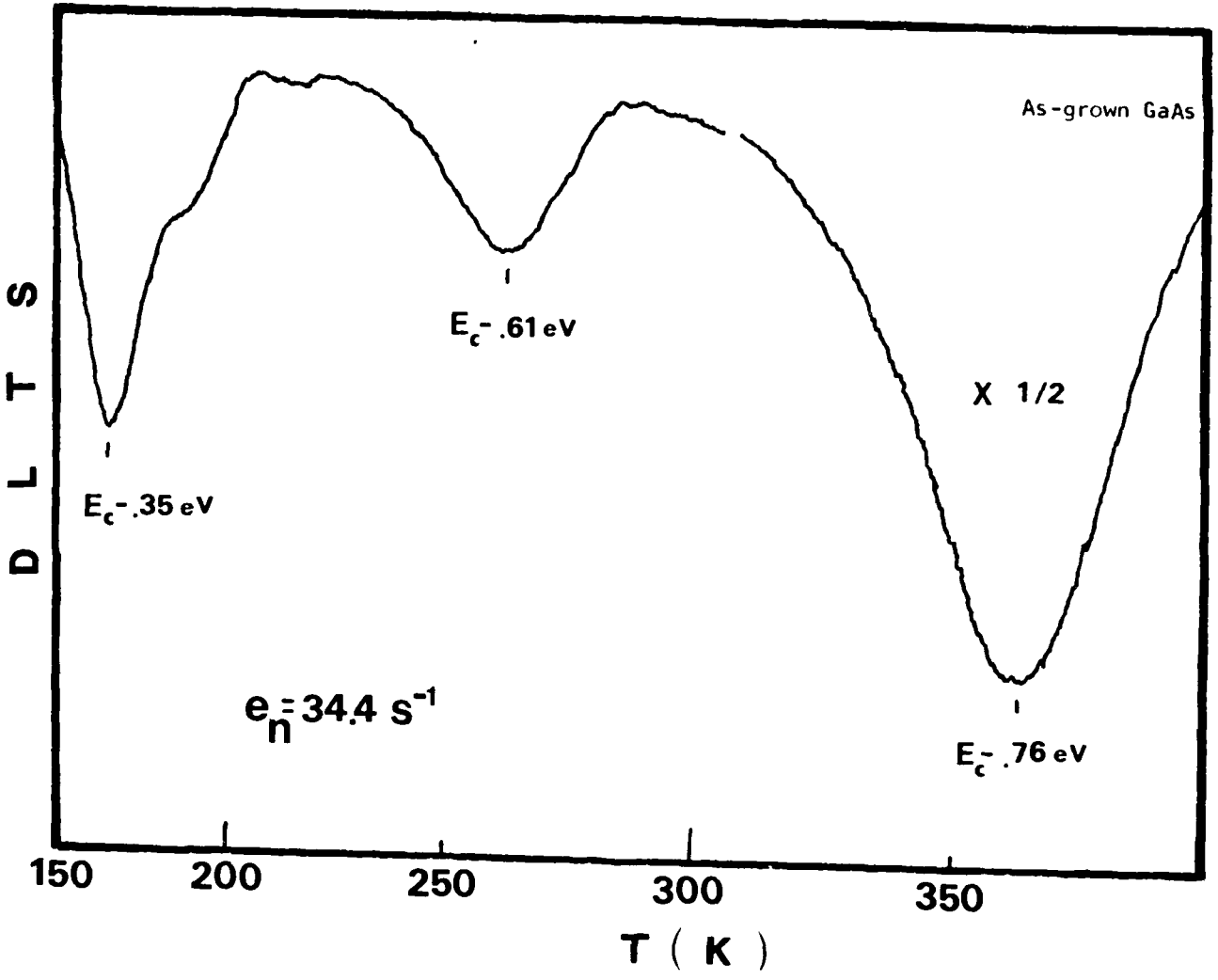

Fig. 4.4 DLTS scan of electron traps in the as-grown GaAs specimen.

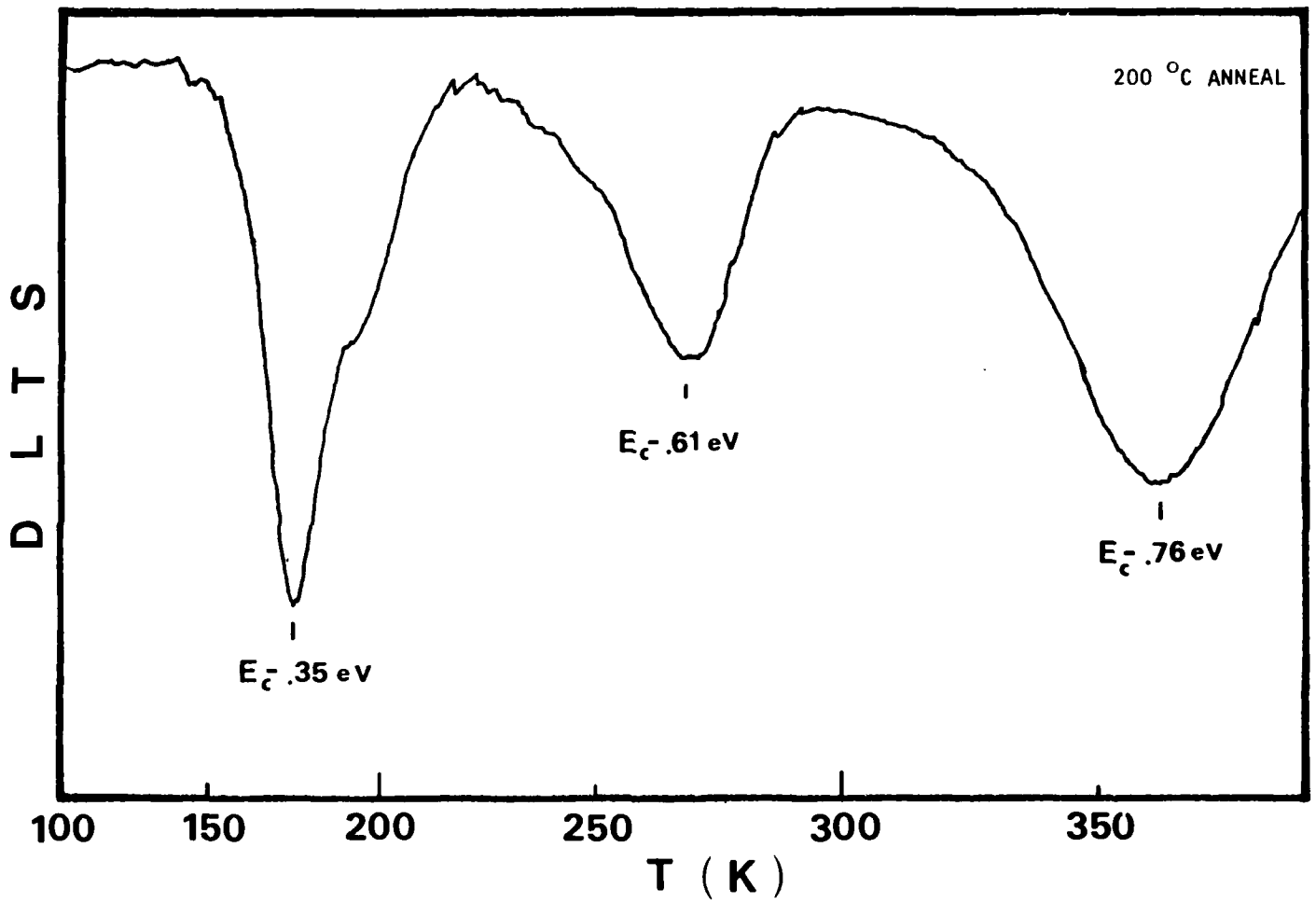

Fig. 4.5 DLTS scan of electron traps in the 200 °C annealed GaAs specimen.

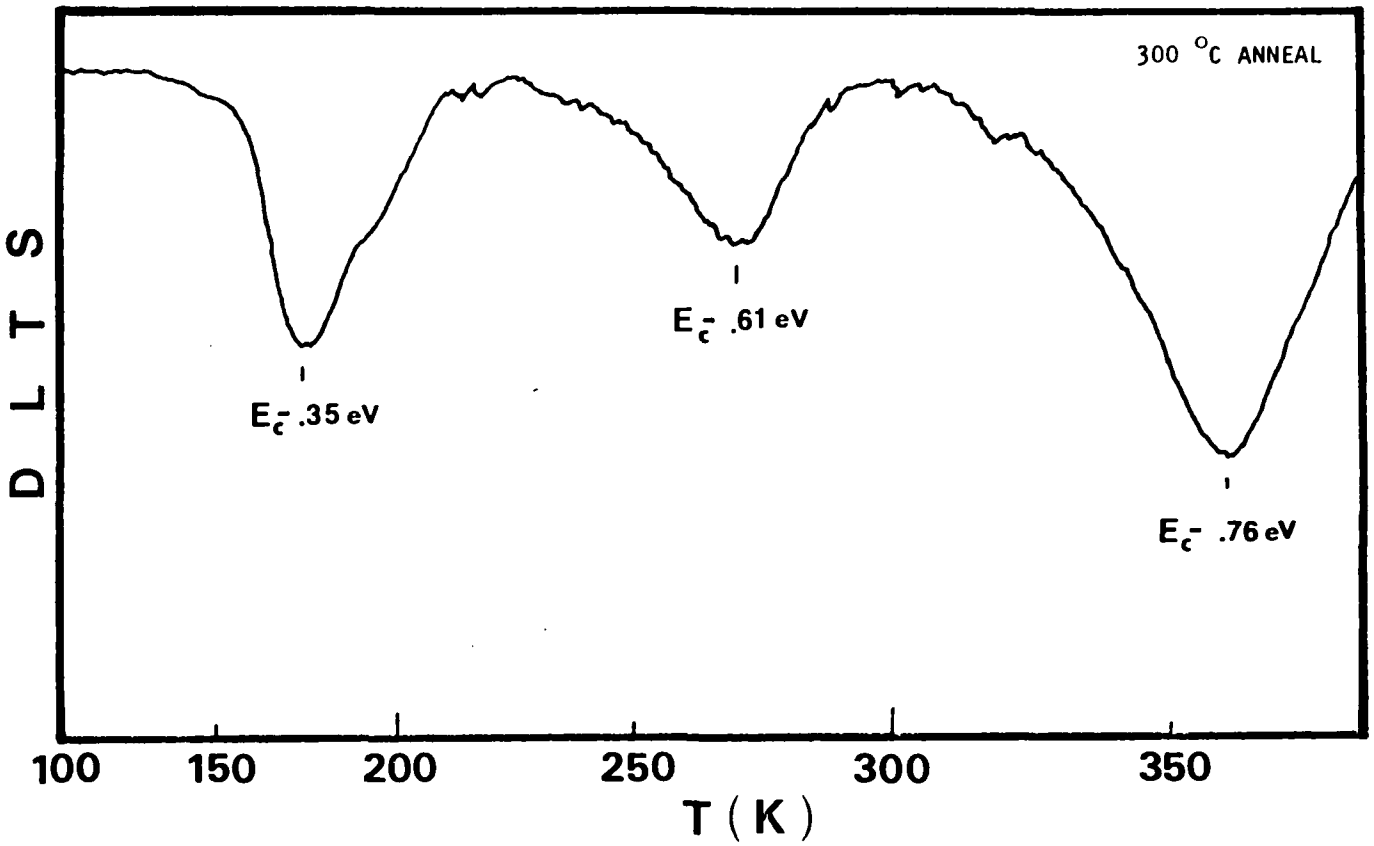

Fig. 4.6 DLTS scan of electron traps for the 300 °C annealed GaAs specimen.

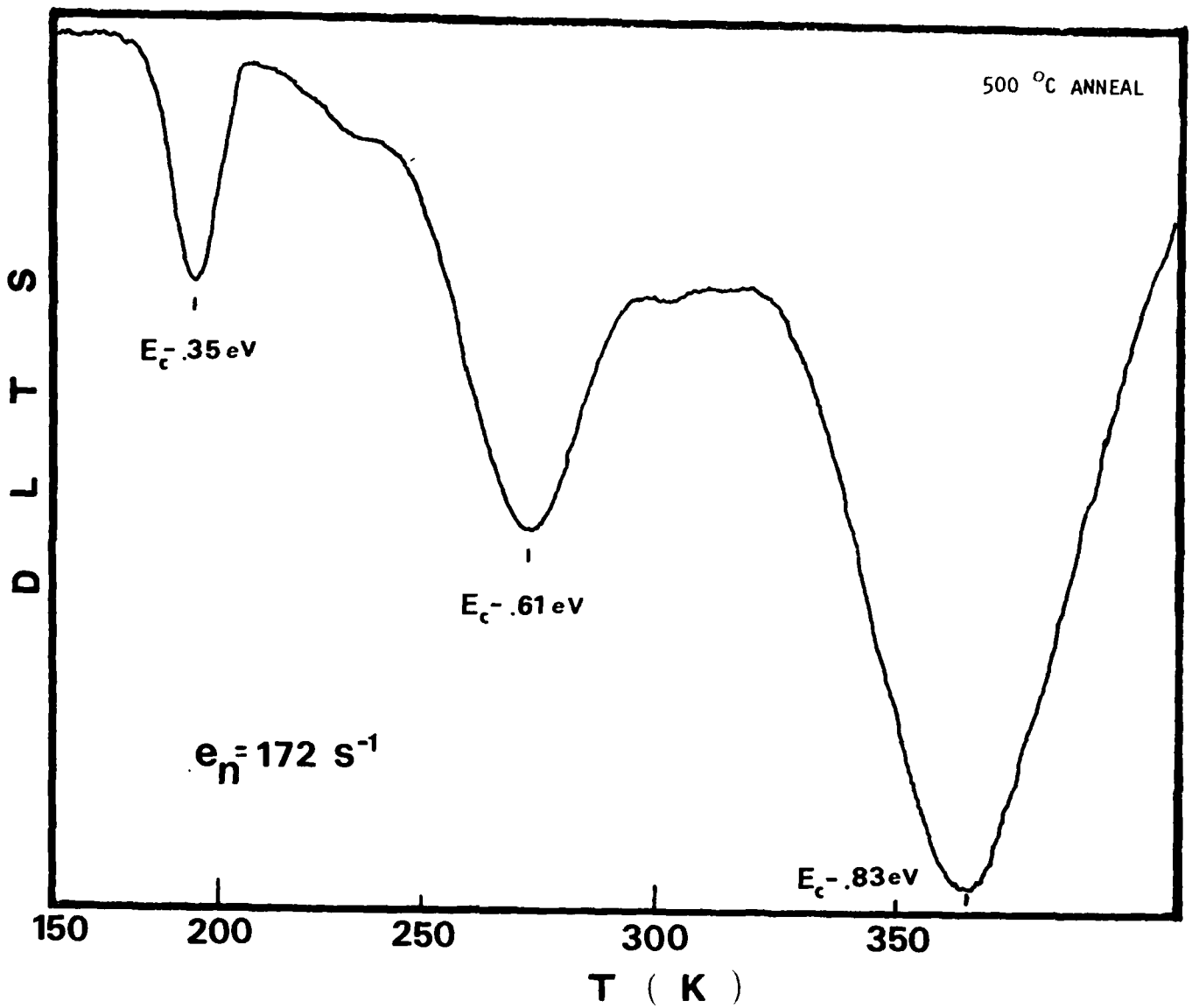

Fig. 4.7 DLTS scan of electron traps for the 500 °C annealed GaAs specimen.

Table 4.3 Defect parameters for the LEC grown GaAs for different annealing temperatures*

Samples	ND(cm-3)	ET(eV)	NT(cm-3)	σn(cm2)
Unanneal	2.5×10^{15}	E1=Ec-0.35	3.8×10^{15}	6.0×10^{-14}
(As grown)		E3=Ec-0.61	3.7×10^{14}	1.2×10^{-13}
		E4=Ec-0.76	2.5×10^{15}	7.1×10^{-14}
200 C, H2				
1 hour	5×10^{15}	E1	2.8×10^{15}	-
		E3	1.1×10^{15}	-
		E4	1.5×10^{15}	-
300 C, H2,				
1 Hour	4.3×10^{15}	E1	1.9×10^{15}	-
		E3	5.5×10^{14}	-
		E4	9.8×10^{14}	-
500 C, H2,				
1 Hour	3.3×10^{15}	E1	5.4×10^{14}	-
		E3	3.7×10^{14}	-
		E5	3.6×10^{14}	7.1×10^{-14}

* Annealing performed in H2 ambient for one hour.

LEC: Liquid Encapsulated Czochralski technique.

while the Ec - 0.76 eV level disappearing from the DLTS spectrum; this is shown in Fig. 4.7 for the 500 C annealed sample. The E1 = Ec-0.35 eV level is the main electron trap observed in these LEC grown GaAs samples. This electron trap has also been reported by Martin et al. and Mircea et al. in the bulk GaAs and by Fairman et al. in the VPE grown GaAs buffer layer. The reduction in free carrier density with increasing annealing temperature along with large capture cross section for these electron traps indicating that they are acceptor type electron traps. Fig.4.8 and Fig.4.9 show respectively the Arrhenius plots for the E1, E5, E3, and E4 traps discussed above. Another interesting study on these traps is concerned with the spatial dependence of the defect density for each electron trap ; this is obtained by performing the bias dependence of the DLTS scans, and the results are illustrated in Fig.4.10 and Fig.4.11. From the DLTS scans as a function of the reverse bias voltage, the spatial dependence of trap density is determined for each electron trap. Fig.4.12 to Fig.4.15 show the spatial dependence of the electron traps observed in the as-grown GaAs sample as well as samples annealed at 200, 300, and 500 C. It is clearly shown that for all the samples studied here, the defect density is highest at the surface, and decreases as it moves away from the interface of the metal-GaAs Schottky contact; the trap density becomes constant deep into the bulk region (i.e., 2 um or deeper) of the GaAs substrate, indicating that all these electron traps are bulk related defects. Mircea et at have also observed a similar defect density profile for the E3 level

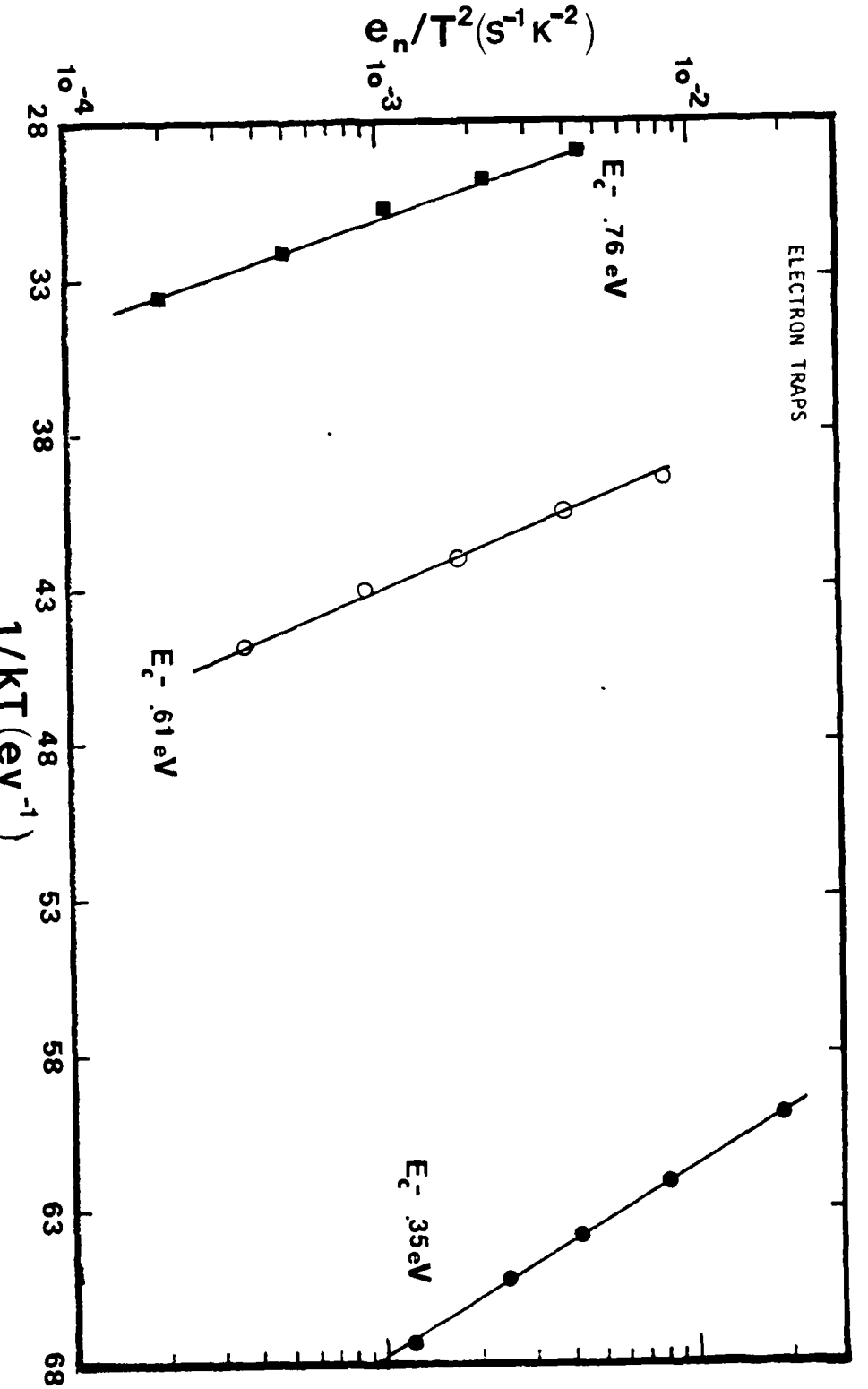

Fig. 4. 8 The Arrhenius plots of three electron trap levels observed in the LEC grown GaAs specimens.

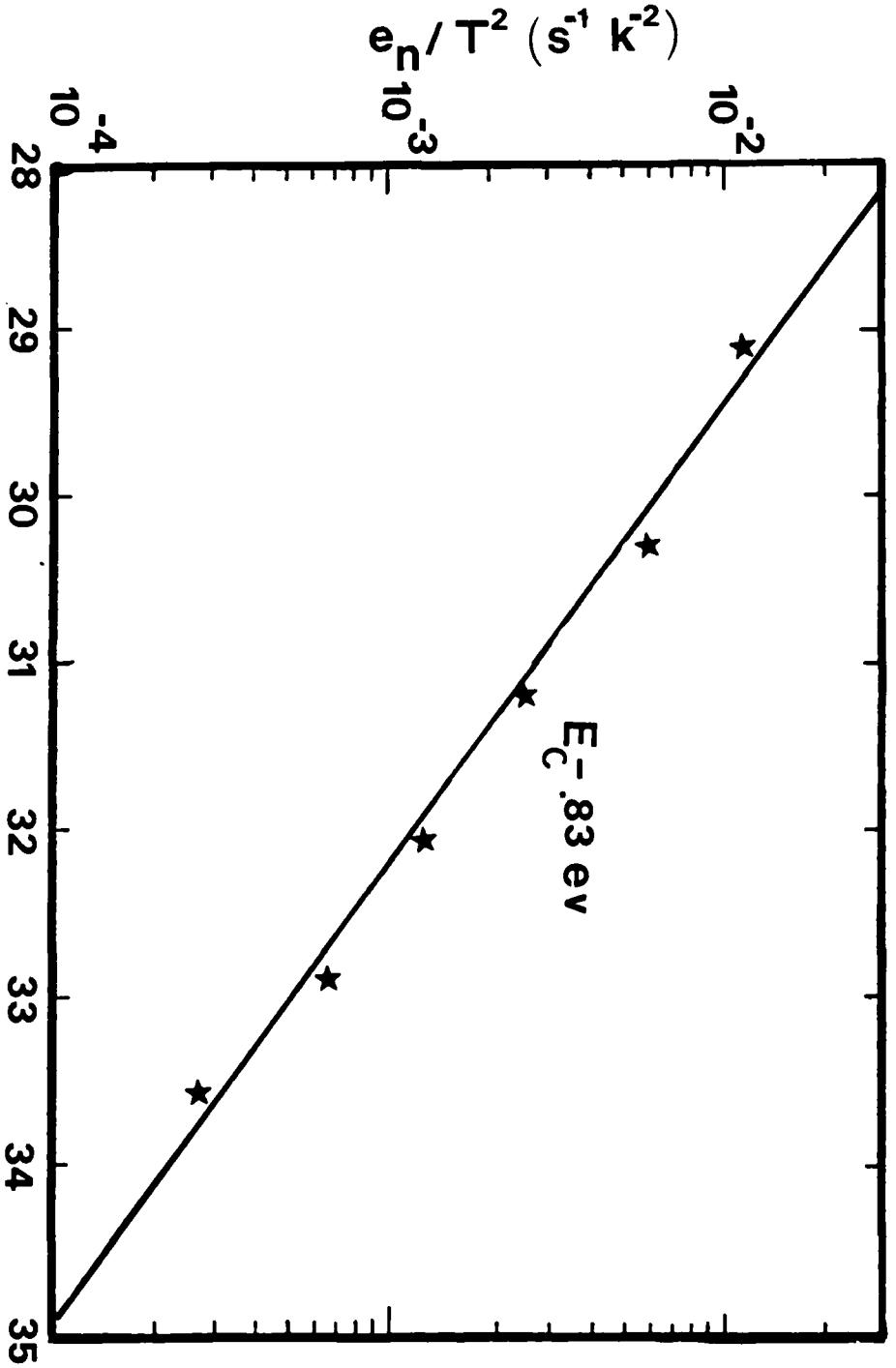

Fig. 4.9 The Arrhenius plot of electron trap (EL2) for the 500 ^{o}C annealed GaAs.

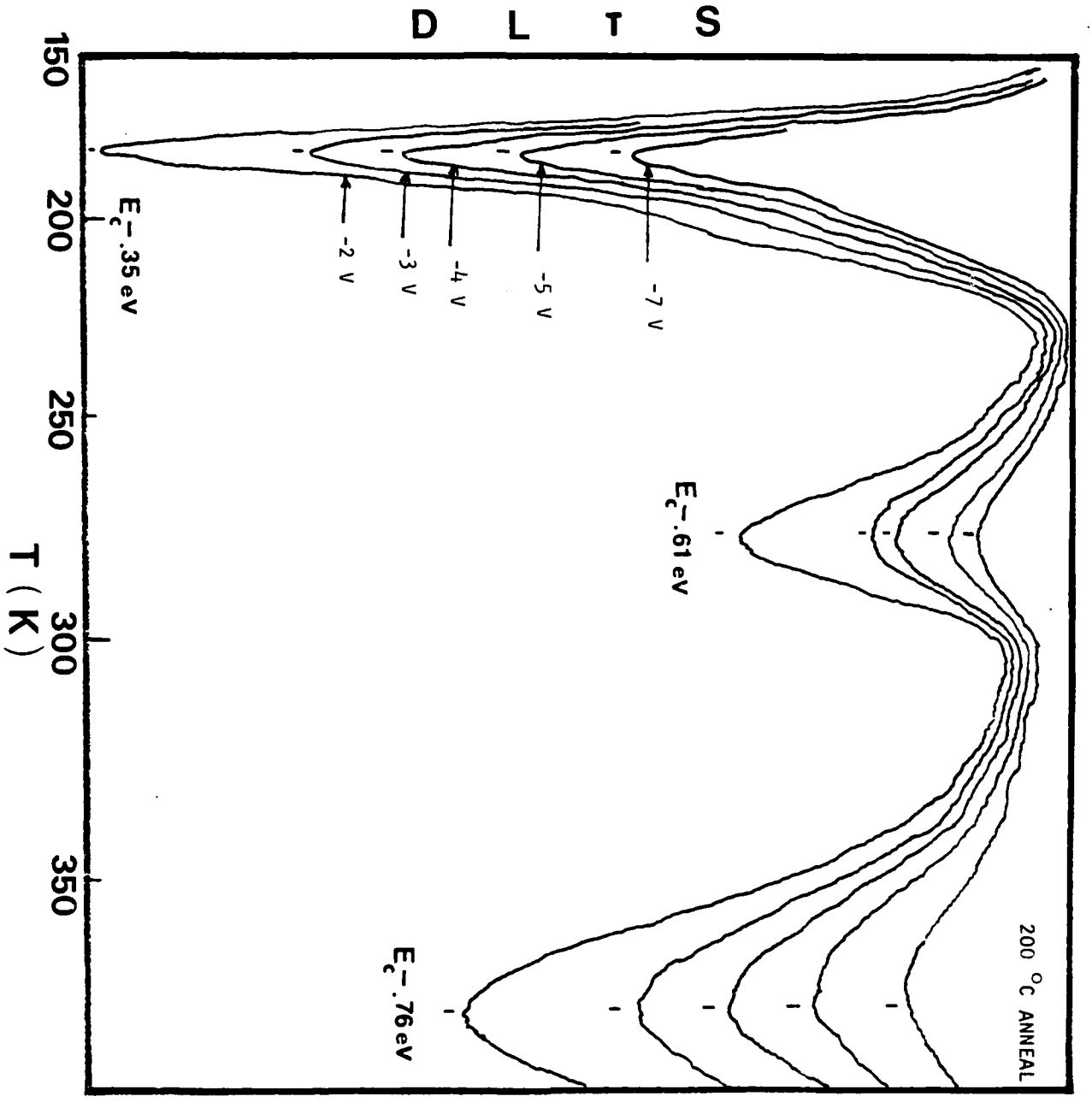

Fig. 4.10 DLTS scans of electron traps for GaAs sample under different reverse bias conditions.

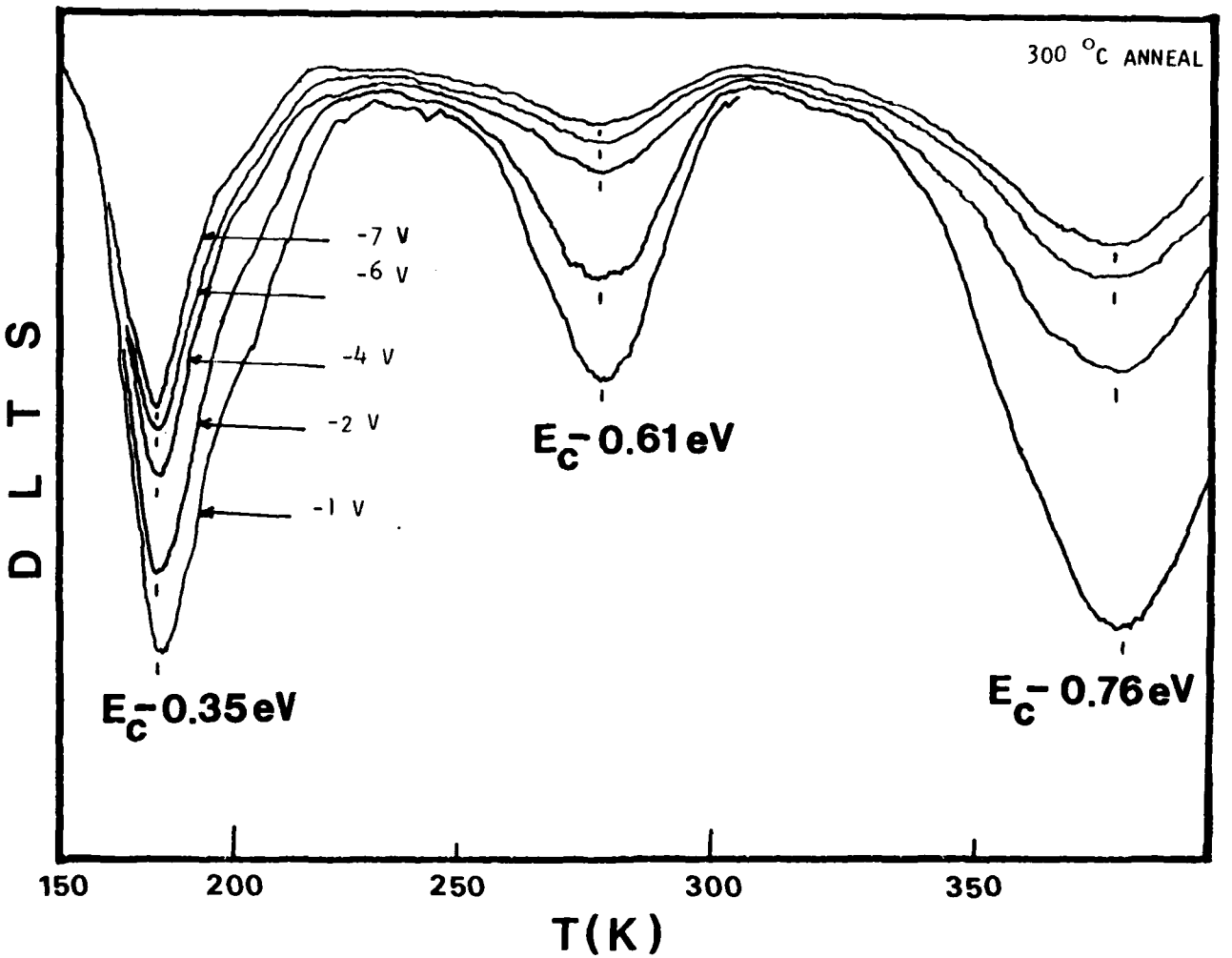

Fig.4.11 DLTS scans of electron traps for the 300 °C annealed GaAs under different bias conditions.

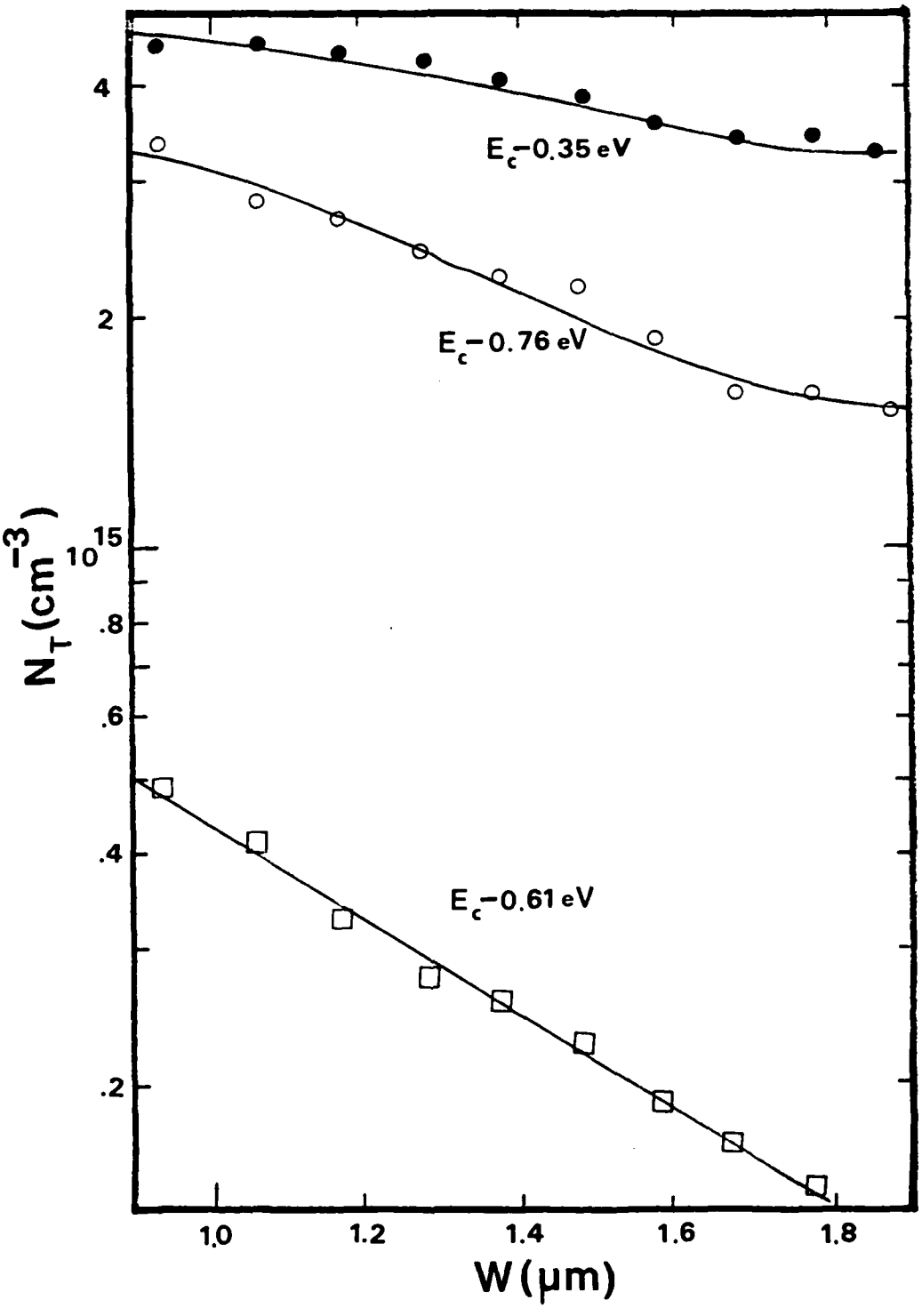

Fig. 4. 12 Density of electron traps vs depletion width in the as-grown GaAs sample.

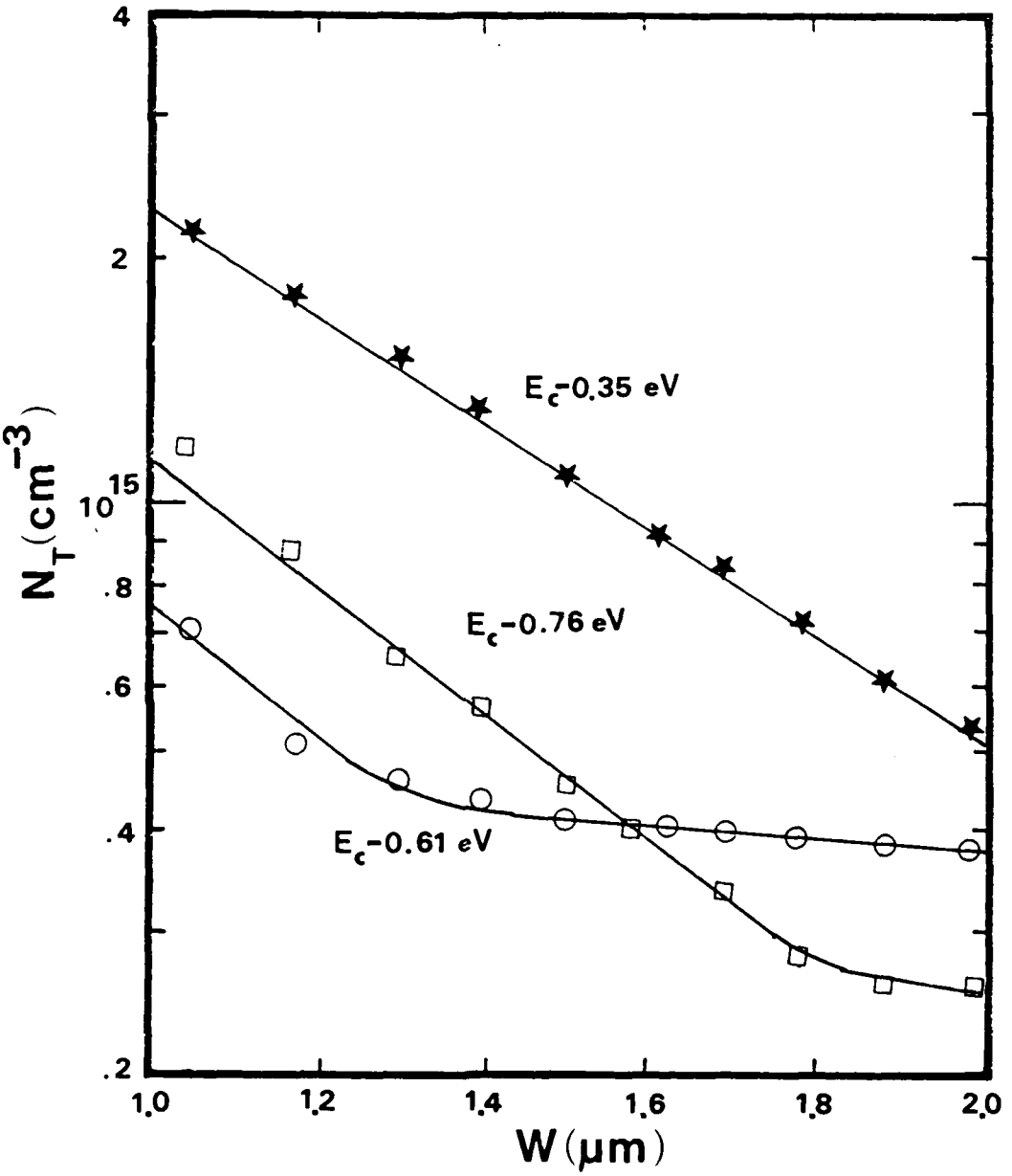

Fig. 4.13 Density of electron traps in the 200 °C annealed GaAs sample as a function of depletion layer width.

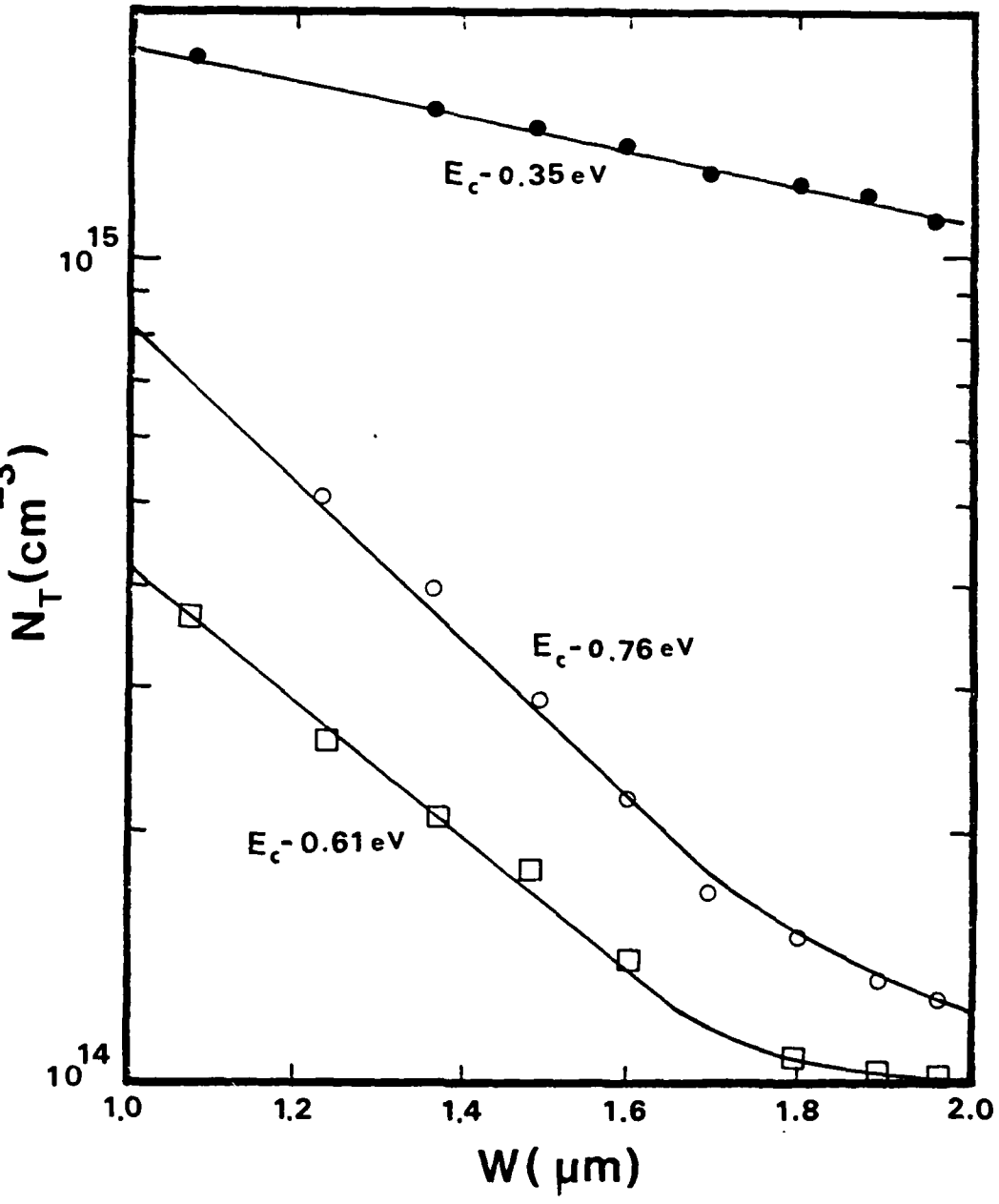

Fig. 4. 14 Density of electron traps vs depletion layer width in the 300 °C annealed GaAs sample.

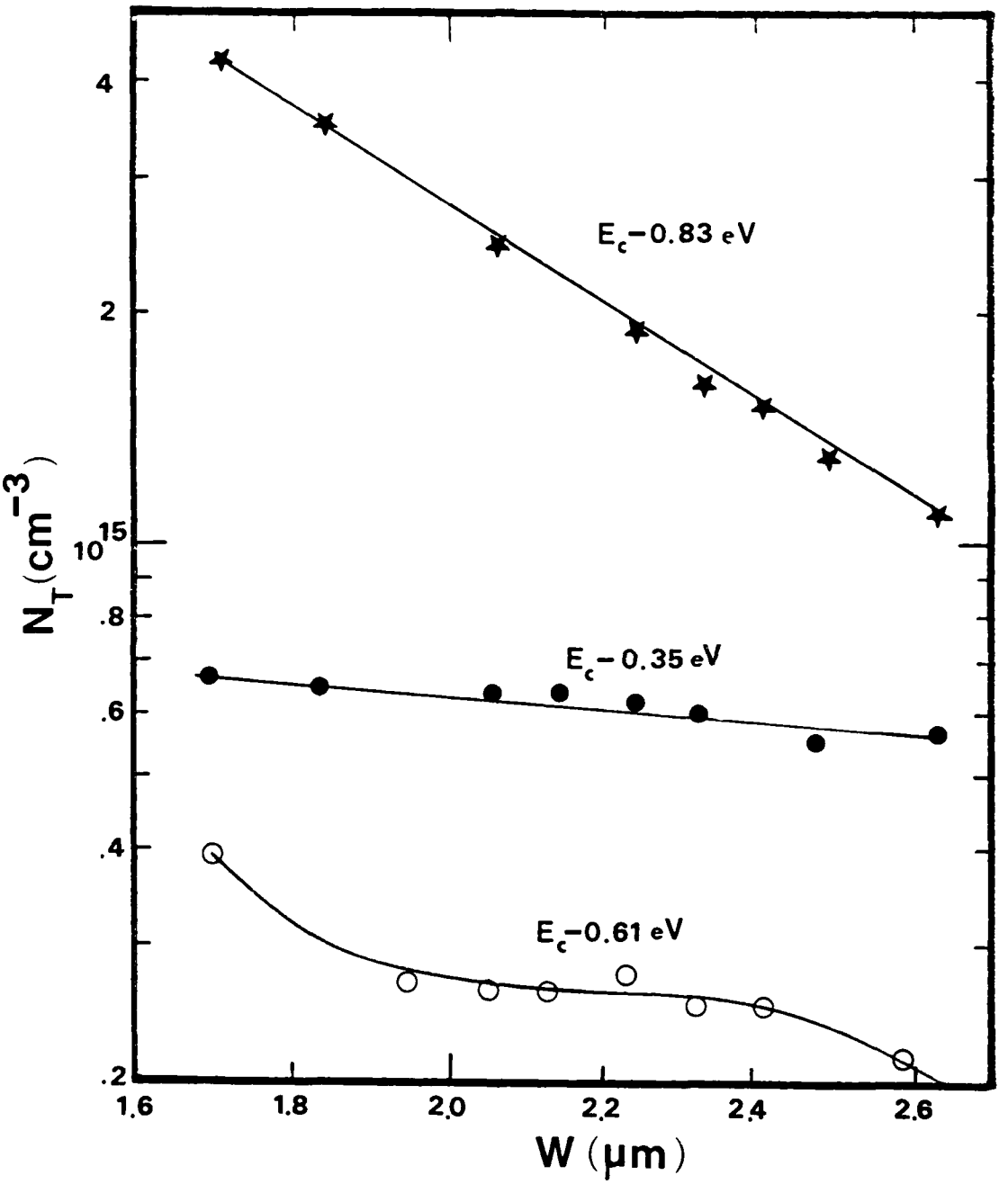

Fig. 4. 15 Density of electron traps vs depletion layer width for the 500 ^{o}C annealed GaAs sample.

in which the density of E3 was increased by the mechanical damage near tne surface of the GaAs specimen.

Our DLTS results (see Table 4.3) showed that the density of the E1, E3 and E4 electron traps was decreased with increasing annealing temperature, while E4 electron trap was annealed out followed by a 500 C H2 annealing for one hour. Recently, Day has observed the E1 and E4 electron traps in the MBE grown n-GaAs, and found that both E1 and E4 electron traps can be annealed out at 800 C for 1/2 hour, or 700 C for one hour. This result suggested that both E1 and E4 electron traps may be due to simple point defects such as vacancy or antisite related defects. The annealing behavior of E1 and E4 electron traps observed here also agreed well with the earlier observation by Cho et. al.

The most noticeable difference between the 500 C annealed sample and the rest of the samples studied is the emerging of the EL2 (Ec-0.83 eV) electron trap in the 500 C annealed sample. The EL2 trap level is the most commonly observed defect in the VPE grown GaAs, its origin is believed to be due to the Ga-vacancy related defect or Ga(As) antisite defect. Day et al. found that the density of EL2 trap would increase with increasing annealing temperature and annealing time for temperatures greater than 500 C. This may be explained in terms of the out-diffusion of the host atoms, presumably gallium, resulting in the creation of vacancy related defect at high annealing temperature. Additional study is currently being undertaken to find out the transition temperature in which the EL2 level is formed in the GaAs.

4.3 Native Defects in the MOCVD grown n-GaAs on Semi-insulating GaAs and Ge Substrates

Characterization of native defects in n-GaAs epitaxial layers grown on semi-insulating GaAs and germanium substrates by the MOCVD technique has been made using the Schottky diode structure. The Sn-doped GaAs epilayer on SI GaAs substrate was grown at 700C for 30 minutes with Ga/As ratio of 11/1, and the dopant density for this sample, as determined by the C - V measurement, was found to be 4.1xE17 cm-3. As for the Sn-doped GaAs epilayer on S.I germanium substrate, the sample was prepared at 706 C for 30 minutes with Ga/As ratio of 7/1; the background dopant density was found to vary between 1xE16 to 1.9xE17 cm-3. The DLTS measurement was performed on both samples, and the results are shown in Fig.4.16 and Fig.4.19, respectively. Fig.4.16 shows the DLTS scan of electron trap for the n-GaAs epilayer on S.I GaAs substrate. The result shows that there is one electron trap with energy of Ec-0.60 eV and density of 1xE16 cm-3. This electron trap level is corresponding to the E3 level discussed in section 4.2 for the LEC grown GaAs samples. In order to study the nature of this electron trap, the field dependence of the capture cross for this electron trap was measured by the DLTS experiment and the result is illustrated in Fig.4.18. The result shows that the capture cross section for this electron trap increases linearly with increasing electric field strength; this indicates that the Ec - 0.60 eV level is a donor type defect center. Furthermore, laser annealing (50 mW CW argon laser) on this GaAs specimen showed that the density of this electron trap decreased slightly

after 8 minutes annealing and the peak of the DLTS scan also shifts to the higher temperature region. This is clearly shown in Fig. 4.19. As for the GaAs epilayer on S.I germanium substrate, the DLTS scan showed a total different defect spectrum; no electron trap was observed in this sample. Instead, a hole trap with energy of Ev + Ø.75 eV and density of 1.7xE13 cm-3 was observed in this sample; this is shown in Fig.4.17. The distinct difference in the defect spectrum observed in these two samples is quite interesting and deserved further investigation. The most likely reason for causing such a change in defect spectrum is not clear at present, and further study is being undertaken. Since the MOCVD grwon GaAs epitaxial materials have received considerable attention in recent years due to the importance of this technology for fabricating high speed III-V devices, study of the native defects as well as the processing induced defects in this material has also become an important task in our research program. Efforts along this direction will be emphasized over the next research period.

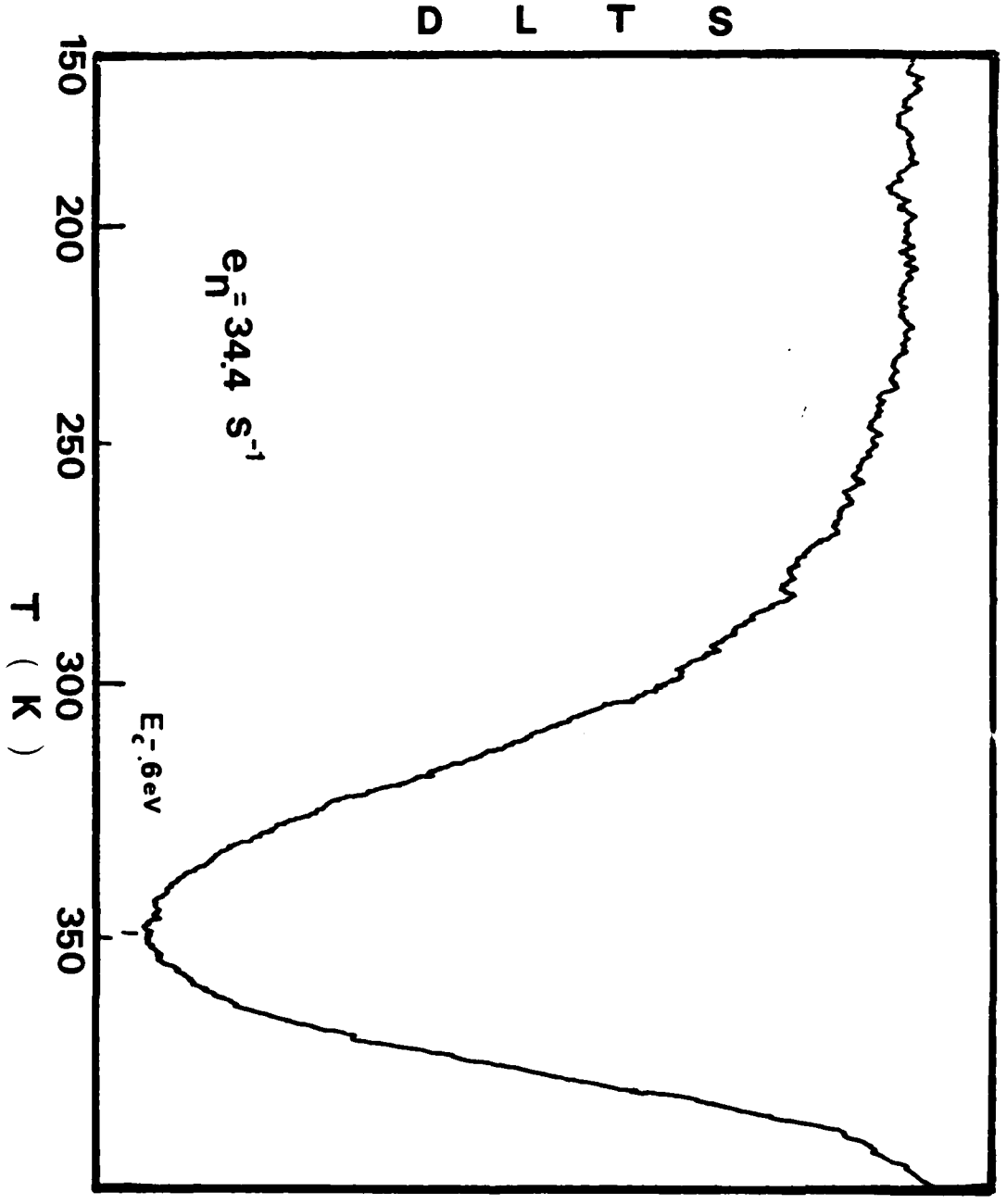

Fig. 4. 16 DLTS scan of electron trap in the MOCVD grown GaAs on S.I. GaAs substrate.

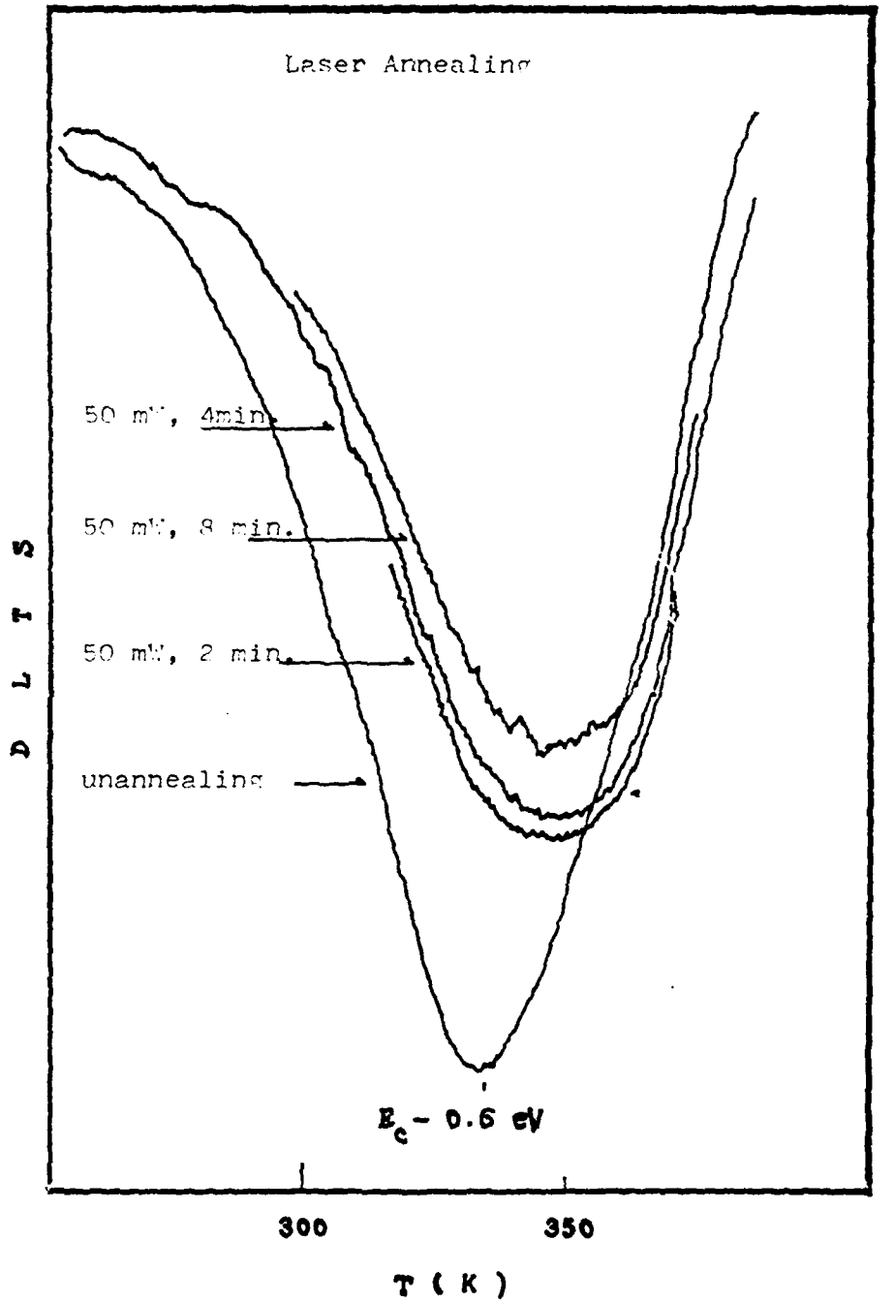

Fig. 4.17 DLTS scans of electron trap as a function of laser annealing time.

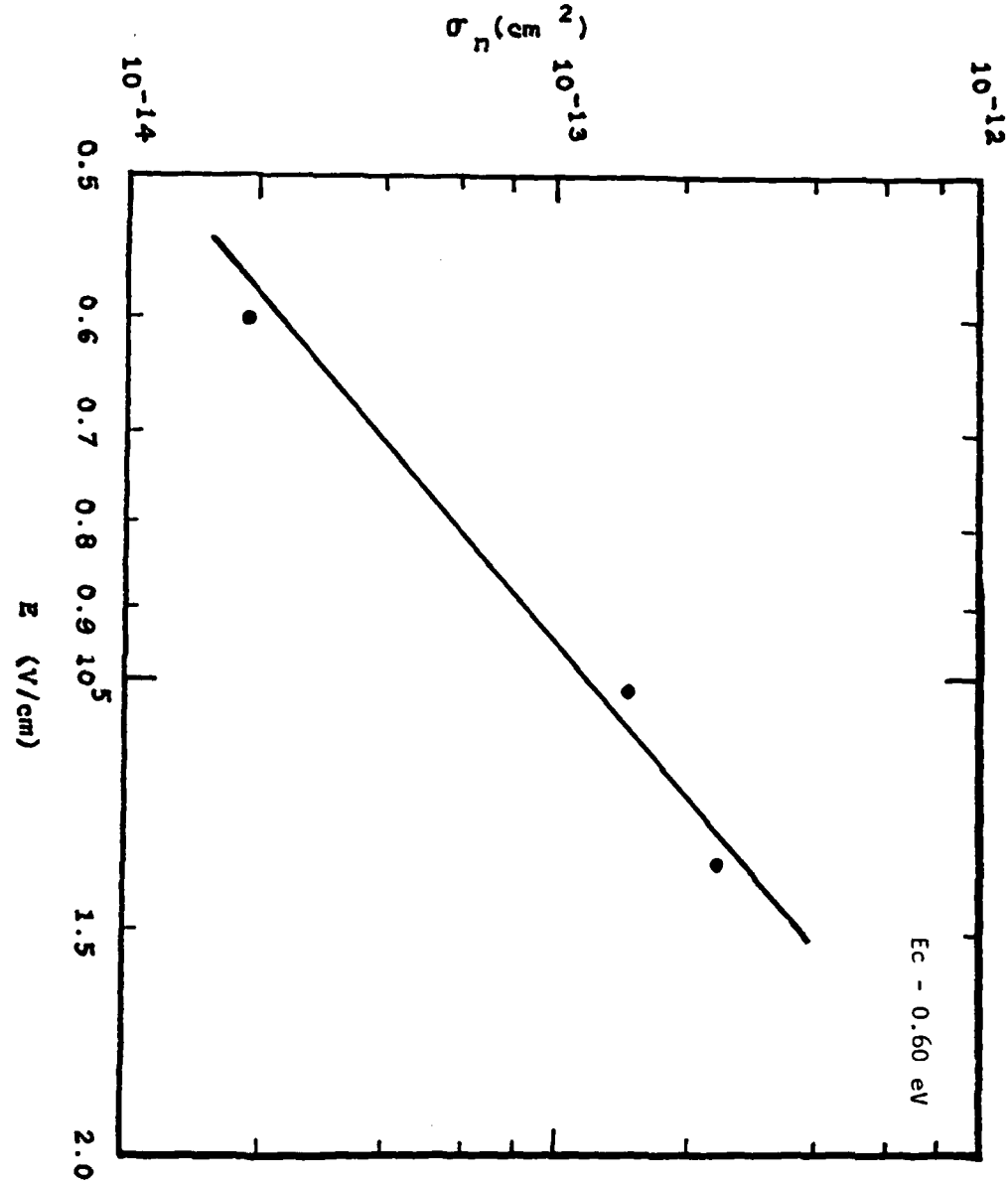

Fig. 4.18 The electric field dependence of electron capture cross section for the Ec-0.60 eV level observed in GaAs epilayer on S.i. GaAs substrate.

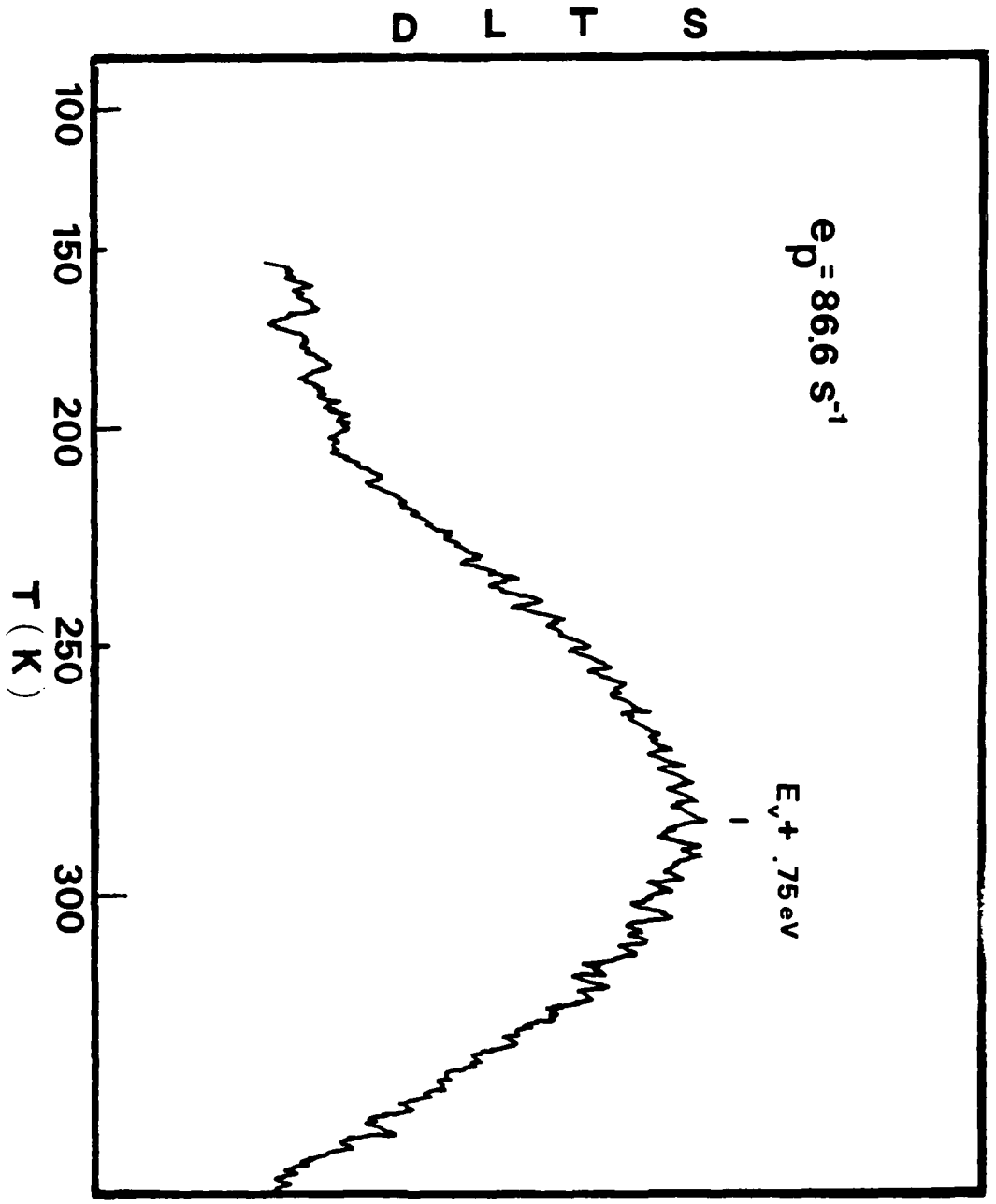

Fig. 4.19 DLTS scan of hole trap in the MOCVD grown GaAs on S. I. germanium substrate.

V. Defect Characterization in One-MeV Electron Irradiated GaAs LPE Layers

5.1 Overview

The GaAs LPE layers used in this study were grown by Dr. Loo at Hughes Research Laboratories (HRL) using infinite solution melt liquid phase epitaxial (LPE) technique. These test diodes have identical device structure (Fig.5. 1) and were processed under identical conditions as the large area (2x2 cm2) GaAs solar cells fabricated by HRL. Study of the effects of one-MeV electron irradiation on the performance of these large area GaAs solar cells has been carried out by Loo et al. Two types of GaAs LPE layers were fabricated for this study: The undoped GaAs with carrier density of 1.5xE15 cm-3 and the Sn-doped GaAs with dopant density of 5xE16 cm-3. For the Sn-doped GaAs, one-MeV electron irradiation was performed at room temperature for fluences of 1xE14, 1xE15, and 1xE16 cm-2, and were subsequently annealed at 230 C for 10, 20, 30, and 60 minutes. In addition, irradiation was also made on the Sn-doped GaAs for fluxes of 2xE9 and 4xE10 e/cm2-s., for a total fluence of 1xE15 e/cm2 and at 150 and 200 C sample temperature. As for the undoped GaAs ,electron irradiation was performed at 200 C, for fluences of 1xE14 and 1xE15 e/cm2, and at room temperature for electron fluences of 1xE14, 1xE15, 5xE15, and 1xE16 e/cm2. The DLTS, the capacitance-voltage (C-V), and current-voltage (I-V) measurements were used to determine the deep-level defects and recombination parameters in these one-MeV electron irradiated GaAs LPE layers, and the results are discussed next.

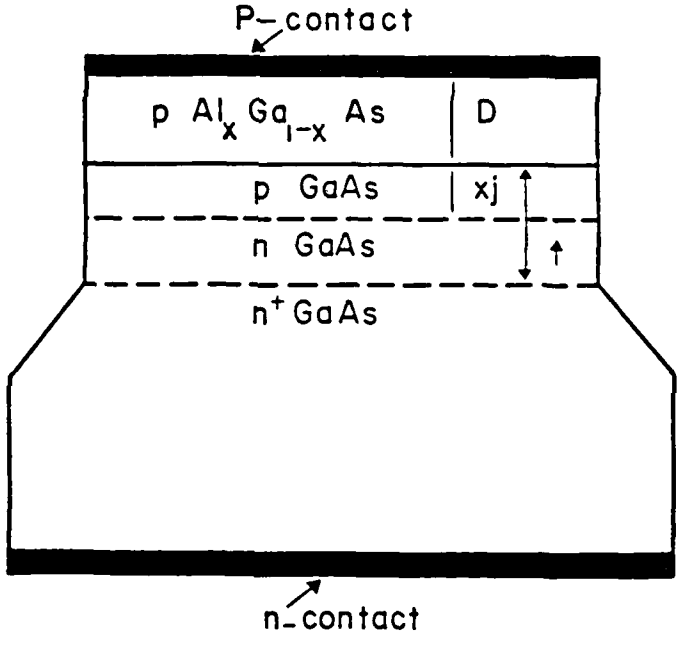

Fig.5.1 Cross sectional view of a GaAs Mesa diode used in the study of one-MeV electron radiation-induced defects in n-GaAs LPE layers.

5.2 Sn-doped GaAs LPE layers irradiated at room temperature and post annealed at 230 C :

The forward I-V characteristics for three Sn-doped GaAs diodes are shown in Fig.5. 2 for electron fluences of zero, 1xE15, and 1xE16 e/cm2. The results showed that forward current is increased with increasing electron fluence in these irradiated GaAs diodes.This result is consistent with the DLTS data in which the defect density was also found to increase with increasing electron fluence. The result can be interpreted by the fact that forward current in these electron irradiated GaAs diodes is dominated by the recombination current in the base as well as the junction space charge region of the diodes.

The DLTS technique provides a fast thermal scan of all the defect levels which are electrically active in the junction space charge region of the diodes. Fig.5. 3 and Fig.5.4 show the DLTS scan of electron and hole traps for the Sn-doped GaAs diodes irradiated at room temperature with 1xE16 e/cm2 fluence, and subsequently annealed at 230 C for 20, 30, and 60 minutes, respectively. Three electron traps with energies of Ec-0.31, 0.71, and 0.90 eV and one hole trap with energy of Ev+0.71 eV were observed in these samples. The DLTS results showed that density of each trap was decreased with increasing annealing time following a 230 C annealing. The results also showed that shallower traps such as E3 level can be more easily annealed out by the low temperature annealing than the deeper trap such as E5 level. Significant reduction in the density of Ev+0.71 eV hole trap was also observed in the 230 C annealed sample, as was shown clearly in Fig.5. 4.

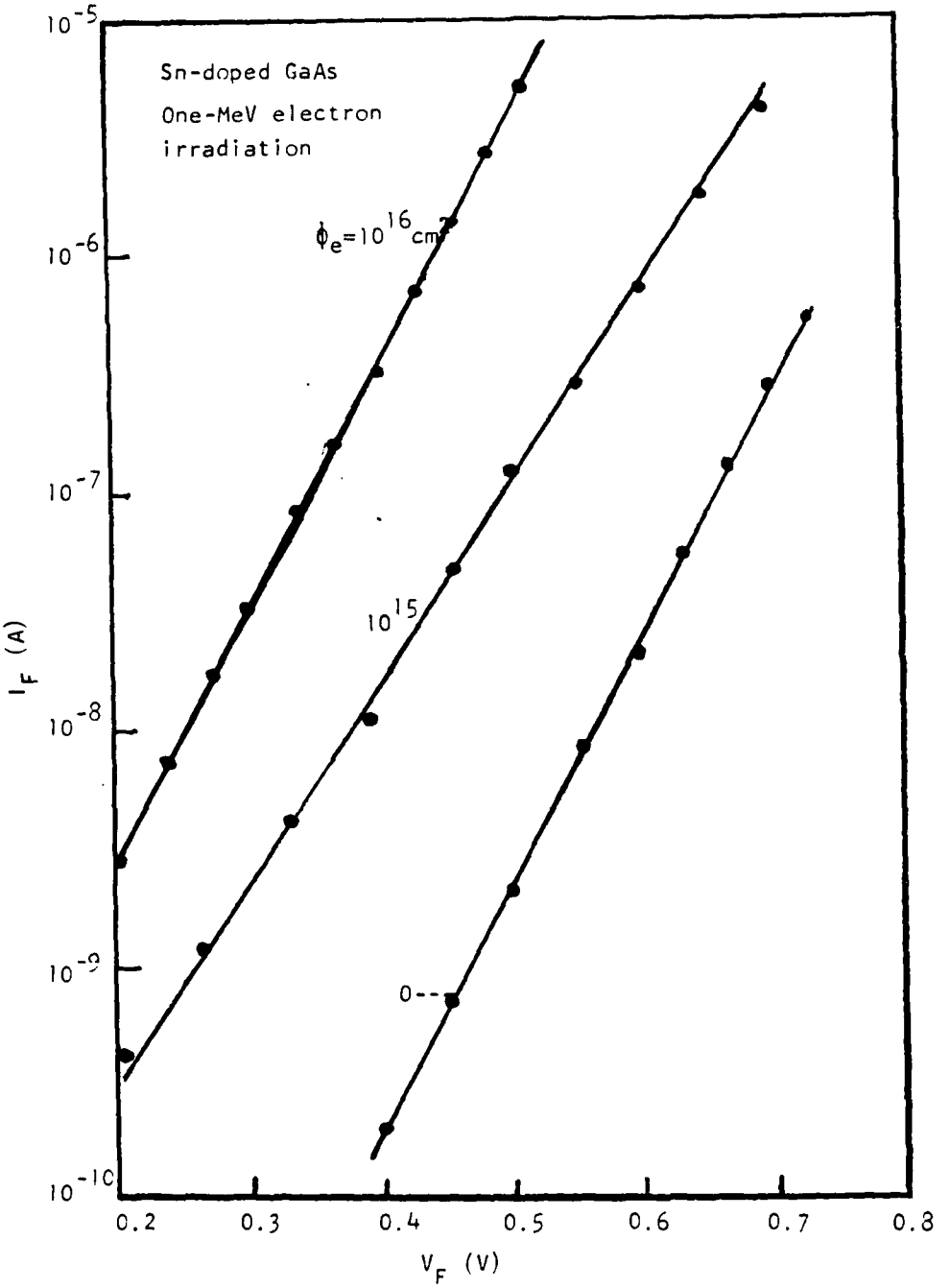

Fig. 5.2 Forward I-V characteristics for one-MeV electron irradiated (AlGa)As-GaAs mesa diodes for different electron fluences.

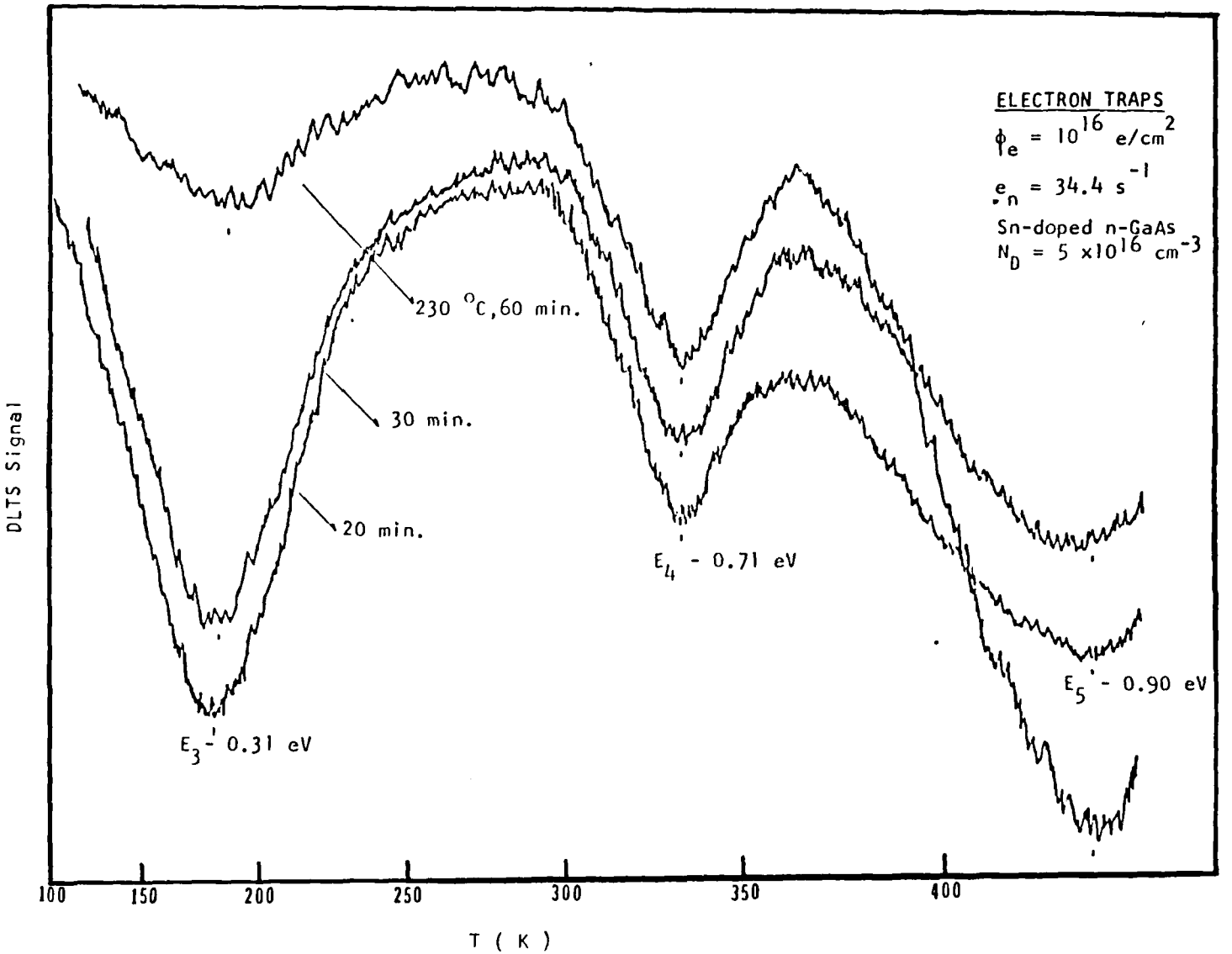

Fig. 5. 3 DLTS scan of electron traps in one-MeV electron irradiated (AlGa)As-GaAs mesa diodes as a function of annealing (230 °C) time.

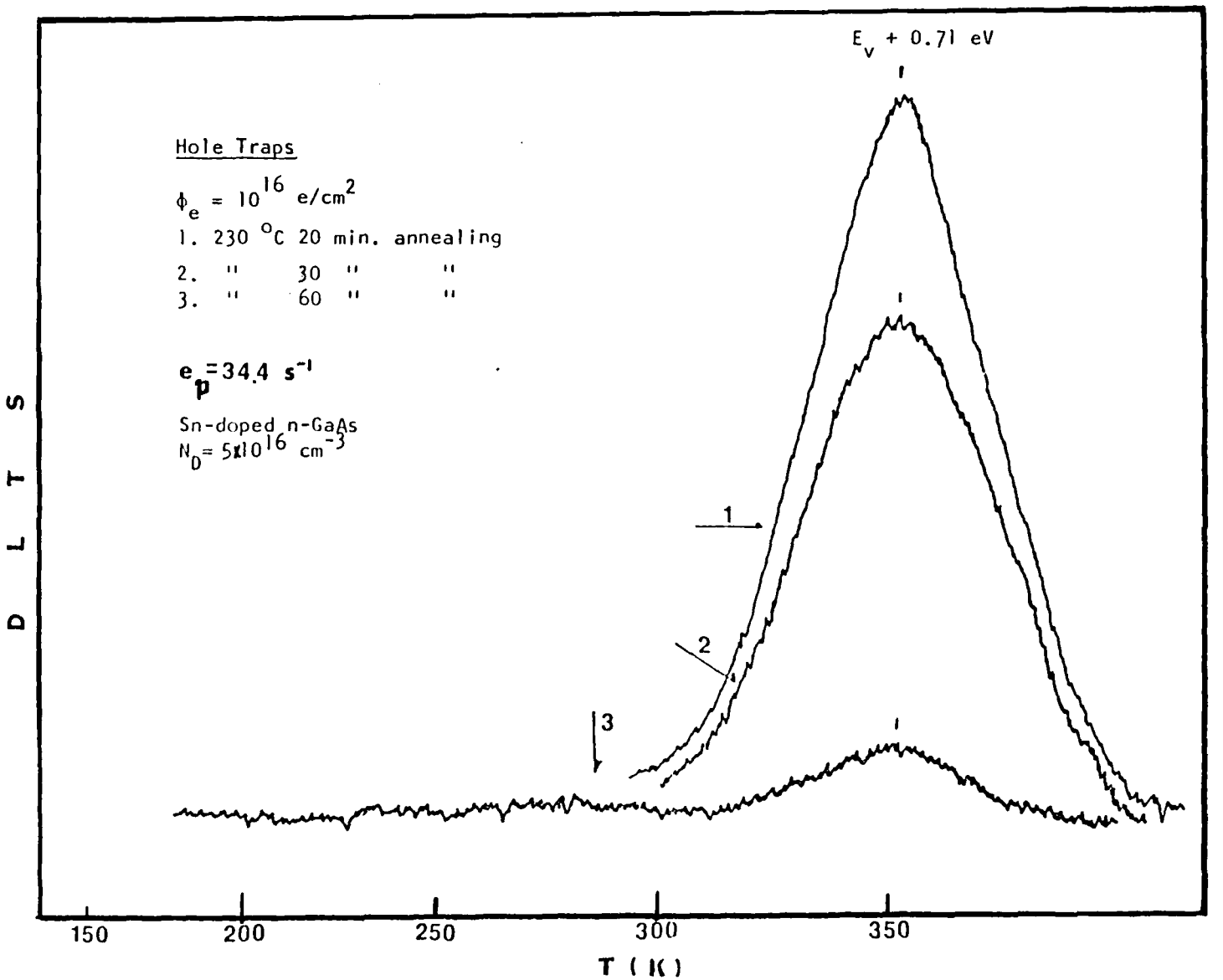

Fig. 5.4 DLTS scan of hole traps in one-MeV electron irradiated (AlGa)As-GaAs mesa diodes for different annealing times.

A similar DLTS result was also obtained for the Sn-doped GaAs diodes irradiated with 1xE15 e/cm2 electron fluence; the results are shown in Fig.5.5 and Fig.5.6. It is noted that the density of each trap level was found to be lower than those samples irradiated with 1xE16 e/cm2 fluence. Table.5.1 and table.5.2 summarize the defect and recombination parameters deduced from the DLTS and C-V data for the Sn-doped GaAs LPE layers discussed above. Note that hole diffusion lengths calculated from the DLTS data were found to vary between 0.5 to 2.5 um, depending on the electron fluence and annealing time used. Fig.5.7 and Fig.5.8 show the defect density vs annealing time for both the electron and hole traps shown in Fig.5.5 through Fig.5.6 for the Sn-doped GaAs annealed at 230 °C for 10 to 60 minutes, respectively. The annealing rate for each trap level can be calculated from the slope of each plot shown in Fig.5.7 and Fig.5.8. For electron traps, the annealing rate is 7.1xE-4 /s for the E3 level for both electron fluences, 3.8xE-4 / s for the E4 level with 1xE15 e/cm2 fluence, 8.3xE-5 /s at 1xE16 e/cm2 fluence, and 1.06xE-3 /s for the E5 level. The annealing rate for the hole trap (Ev+0.71 eV) is 8.6xE-4 /s for 1xE15 e/cm2 fluence and 4xE-5 /s for 1xE16 e/cm2 electron fluence.

5.3 Sn-doped GaAs Irradiated at 150 and 200 C for Two Electron Fluxes and Fluences

To study the effects of varying the flux and the specimen temperature during electron irradiation on deep level defects, irradiation on Sn-doped GaAs diodes was made for fluxes of 2xE9 and 4xE10 e/cm2-s, for a total fluence of 1xE15 e/cm2, and

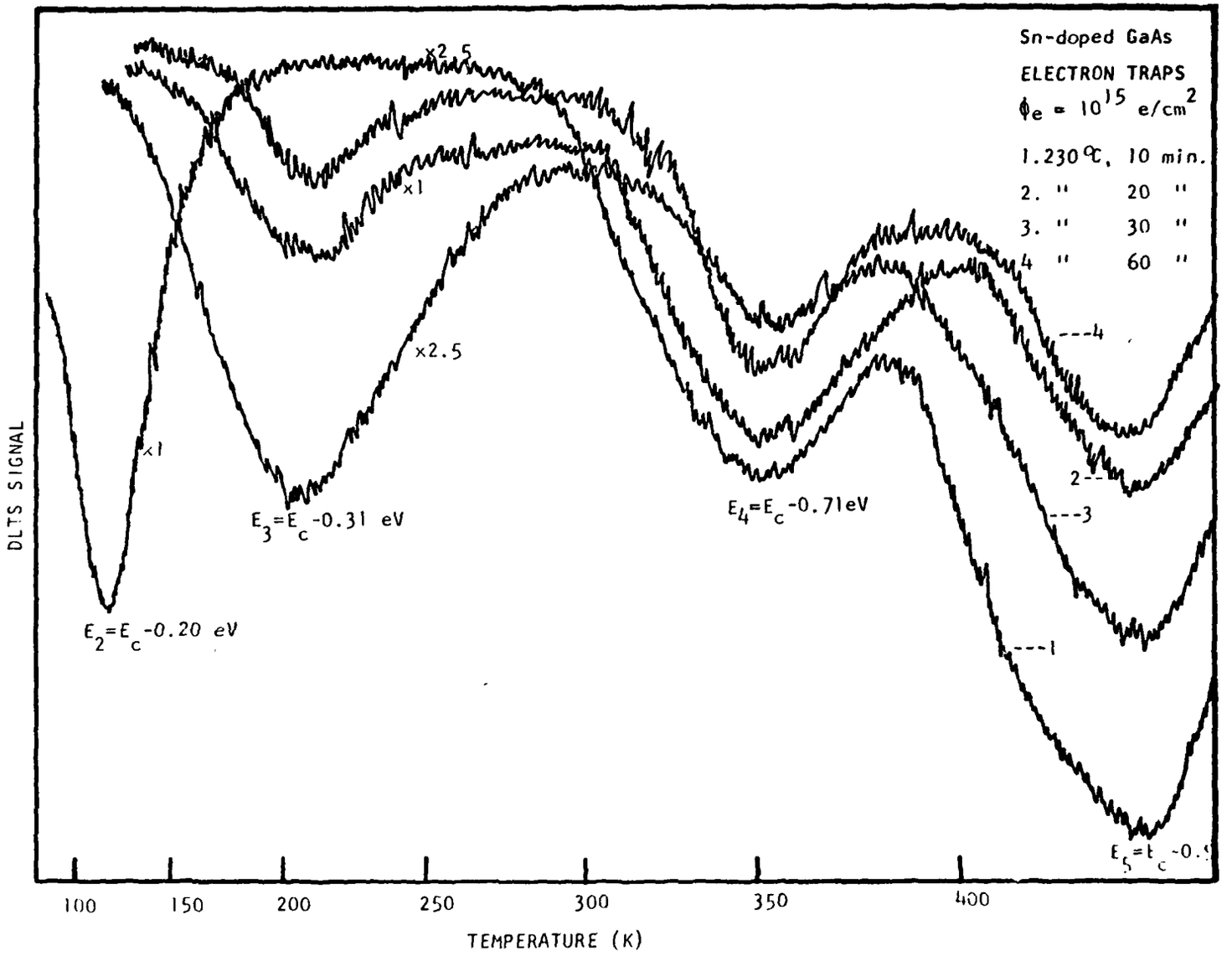

Fig. 5.5 DLTS scan of electron traps in one-MeV electron irradiated (AlGa)As-GaAs mesa diodes vs annealing times for electron fluence of 10^{15} e/cm^2.

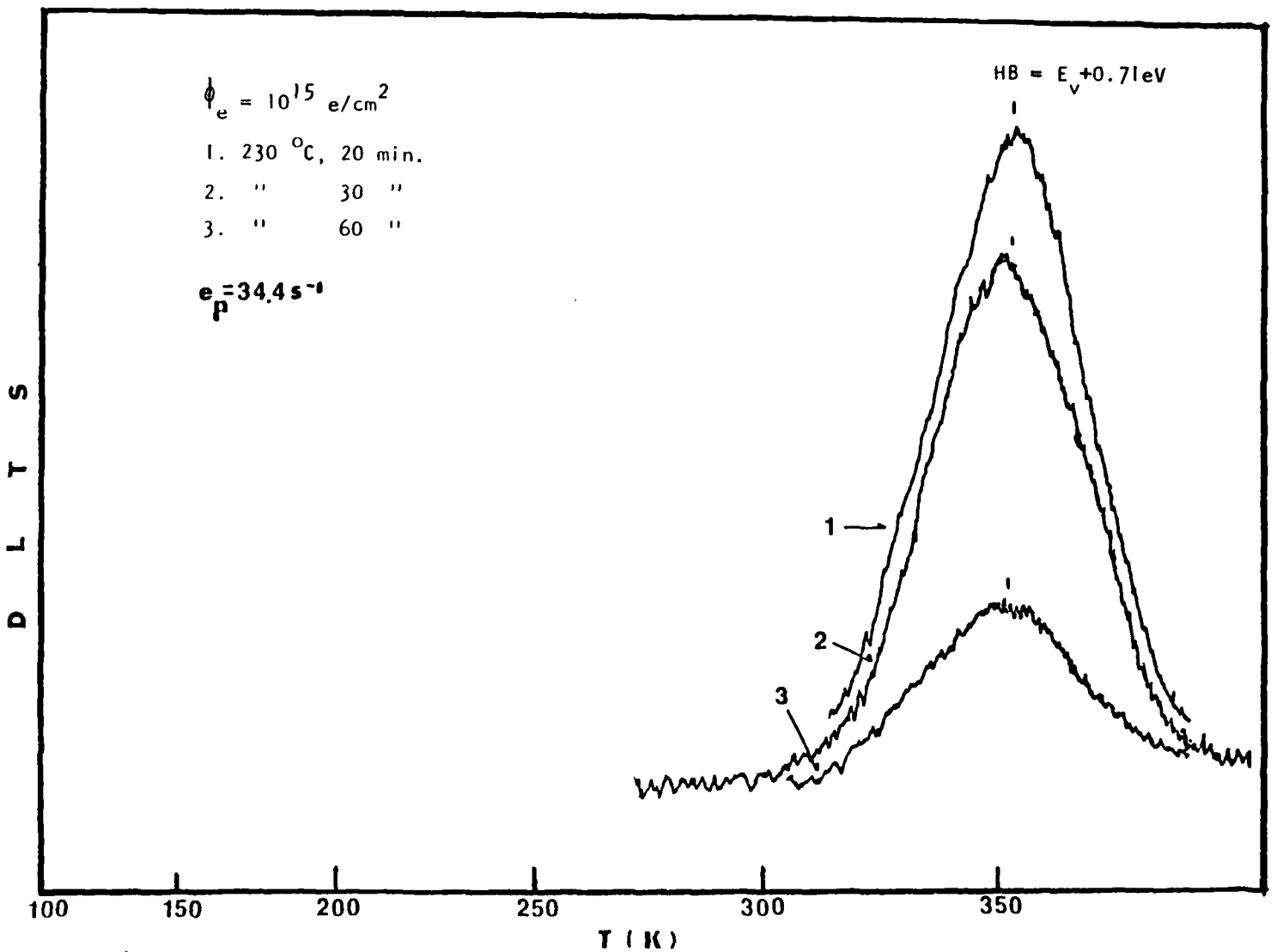

Fig. 5. 6 DLTS scan of hole traps for one-MeV electron irradiated (AlGa)As-GaAs mesa diodes as a function of annealing times for electron fluence of 10^{15} e/cm^2.

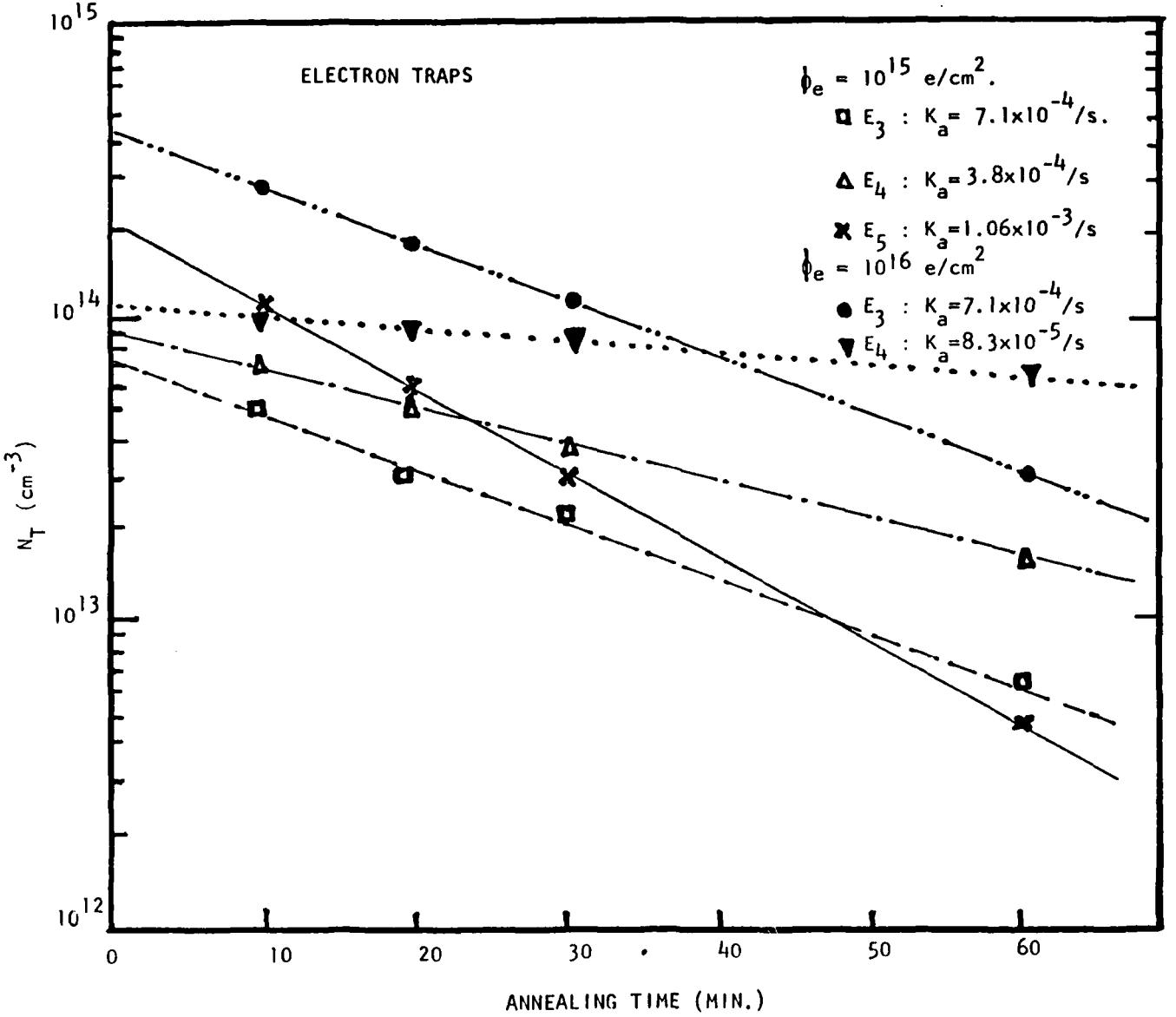

Fig. 5. 7 Density of electron traps vs annealing time in Sn-doped GaAs mesa diodes irradiated by one-MeV electrons. Annealing temperature = 230°C.

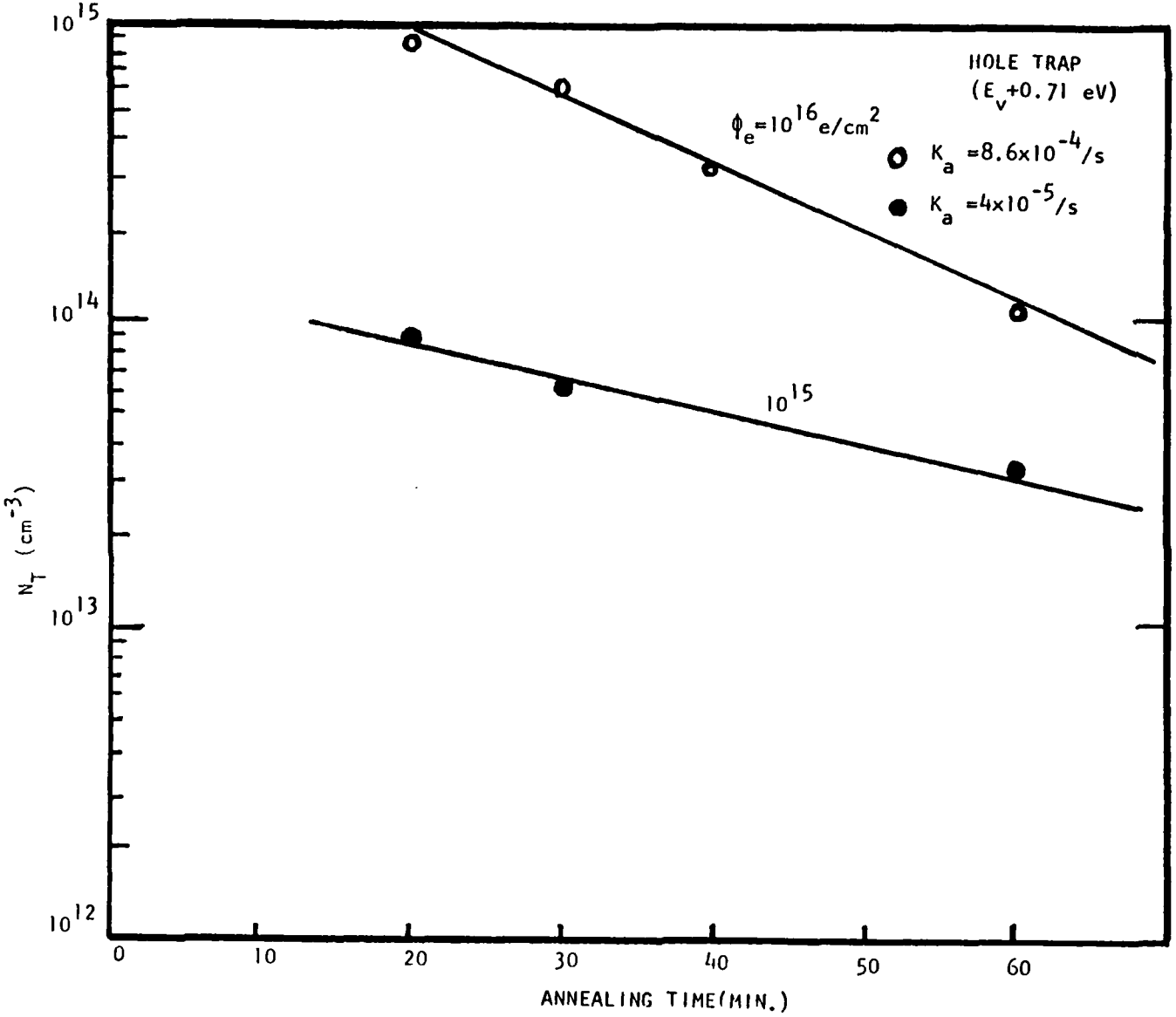

Fig. 5. 8 Density of hole trap vs annealing time for Sn-doped GaAs mesa diodes irradiated by one-MeV electrons. Annealing temperature = 230 ^{o}C.

Table 5.1 Electron trap parameters in one-MeV electron irradiated (AlGa) As-GaAs diodes annealed at 230°C for 10, 20, 30 and 60 min. $N_D = 5 \times 10^{16} cm^{-3}$ (Sn-doped n-GaAs)

Annealing time & Temperature	$\phi_e = 10^{16}$ (e/cm^2)				10^{15} (e/cm^2)			
	E_T (eV)	N_T (cm^{-3})	σ_n (cm^2)	τ_n (s)	E_T (eV)	N_T (cm^{-3})	σ_n (cm^2)	τ_n (s)
Unannealed	$E_2 = E_c - 0.20$	9×10^{12}	1×10^{-16}	2.77×10^{-5}	E_2	7.9×10^{12}	1×10^{-16}	–
	$E_3 = E_c - 0.31$	2.9×10^{14}	1.8×10^{-14}	4.26×10^{-9}	203°C E_3	–	–	–
	$E_4 = E_c - 0.71$	3.2×10^{14}	5.1×10^{-14}	1.25×10^{-9}	,10 E_4	5.7×10^{13}	5.1×10^{-14}	7.64×10^{-9}
	$E_5 = E_c - 0.90$	3.4×10^{14}	5.8×10^{-14}	1.04×10^{-9}	min.) E_5	1.1×10^{14}	5.8×10^{-14}	3.2×10^{-9}
230 C for 20 min.	E_3	1.4×10^{14}	1.8×10^{-14}	9.92×10^{-9}	E_3	2.6×10^{13}	1.8×10^{-14}	4.75×10^{-8}
	E_4	9.5×10^{13}	5.1×10^{-14}	4.39×10^{-9}	E_4	5.4×10^{13}	5.1×10^{-14}	8.07×10^{-9}
	E_5	1.2×10^{14}	5.8×10^{-14}	2.93×10^{-9}	E_5	6.1×10^{13}	5.8×10^{-14}	5.77×10^{-9}
230 C for 30 min.	E_3	1.2×10^{14}	1.8×10^{-14}	1.01×10^{-8}	E_3	2.4×10^{13}	1.8×10^{-14}	5.1×10^{-8}
	E_4	7.7×10^{13}	5.1×10^{-14}	5.41×10^{-9}	E_4	2.5×10^{13}	5.1×10^{-15}	1.6×10^{-8}
	E_5	6.2×10^{13}	5.8×10^{-14}	5.68×10^{-9}	E_5	3.1×10^{13}	5.8×10^{-14}	1.14×10^{-8}
230 C for 60 min.	E_3	2.7×10^{13}	1.8×10^{-14}	4.57×10^{-8}	E_3	7.2×10^{12}	1.8×10^{-14}	5.6×10^{-7}
	E_4	6.2×10^{13}	5.1×10^{-14}	6.45×10^{-9}	E_4	1.8×10^{13}	5.1×10^{-14}	2.22×10^{-8}
	E_5	1.6×10^{14}	5.8×10^{-14}	2.19×10^{-9}	E_5	2.2×20^{13}	5.8×10^{-14}	1.6×10^{-8}

Table 5.2 Electron and Hole Traps in one-MeV Elctron Irradiated (at 200°C) (AlGa)As-GaAs diodes. *

Electorn Fluence ($^e/cm^2$)	N_D (cm^{-3})	Electron Traps		Hole Traps	
		E_T (ev)	N_T (cm^{-3})	E_T (eV)	N_T (cm^{-3})
0	1.5×10^{15}	–	–	–	–
10^{14}	1.45×10^{15}	E_c-0.13	3.2×10^{13}	E_v+0.29	0
		E_c-0.41	1.3×10^{13}	–	–
		E_c-0.71	1.2×10^{12}	E_v+0.71	6.4×10^{12}
		E_c-0.90	1.6×10^{12}	–	–
10^{15}	1.05×10^{15}	E_c-0.13	2.2×10^{14}	E_v+0.29	6.9×10^{12}
		E_c-0.41	1.3×10^{13}	–	–
		E_c-0.71	7.8×10^{12}	E_v+0.71	2.0×10^{13}
		E_c-090	9.5×10^{12}	–	–

*Carrier removal rate - $\Delta n/\phi_e = 0.5\ cm^{-1}$. undoped n-GaAs LPE layer.

isothermal annealing at 150 and 200 C was carried out on these GaAs LPE layers during electron irradiation. Fig.5.9 and Fig.5.10 show the DLTS scans of electron and hole traps for the Sn-doped GaAs irradiated by two different fluxes at 150 and 200 C, respectively. The results show that the dominant electron trap is due to the Ec-0.71 eV level, and the dominant hole trap is due to the Ev+0.71 eV level. Density of both traps was found to increase with increasing incident flux and reducing sample's annealing temperature. It is noted that samples irradiated with 2xE9 e/cm2-s flux has only one electron trap observed as compared to three electron traps for samples irradiated with 4xE10 e/cm2-s electron flux. A significant difference in the DLTS spectrum was also noted when compared the DLTS curves shown in Fig.5.3 with Fig.5.9 for the electron traps. The results clearly indicate that isothermal annealing process used during electron irradiation is as effective in reducing the electron trap density as the post annealing treatment. Table.5.3 and table.5.4 summarize the defect and recombination parameters calculated from the DLTS and C-V data for the Sn-doped GaAs cells irradiated with different fluxes and annealing temperatures.

5.4 Undoped GaAs Irradiated at 200 °C

In addition to the DLTS results shown above for the Sn-doped GaAs, we have also performed electron irradiation on the undoped GaAs at 200 C for electron fluences of 1xE14 and 1xE15 e/cm2. Fig.5.11 shows the forward I-V characteristics for the undoped GaAs irradiated with electron fluences of 1xE14 and 1xE15 e/cm2. The results showed that the forward current was increased with

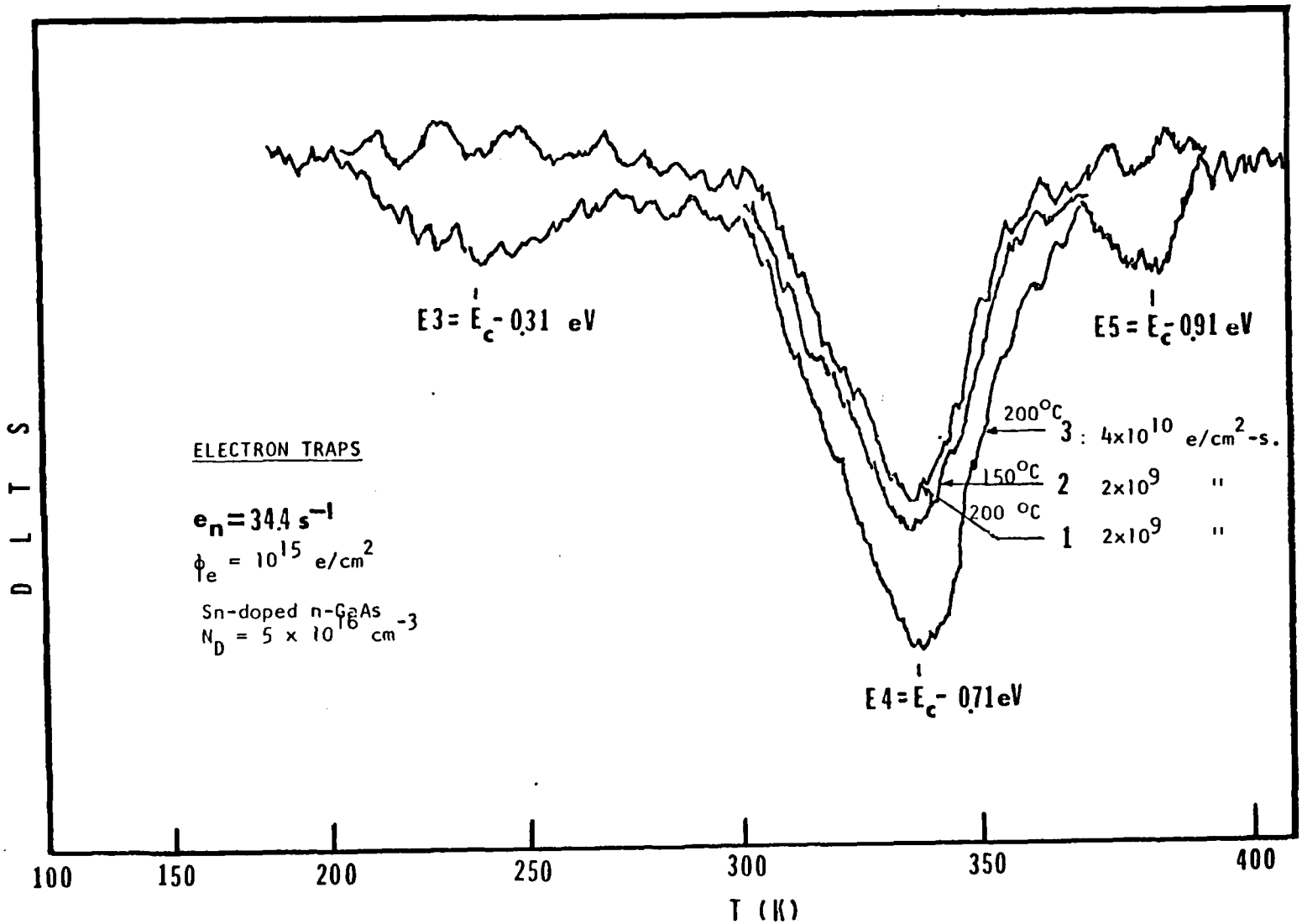

Fig. 5. 9 DLTS scan of electron traps in one-MeV electron irradiated (AlGa)As-GaAs diodes vs incident flux rate and annealing temperature.

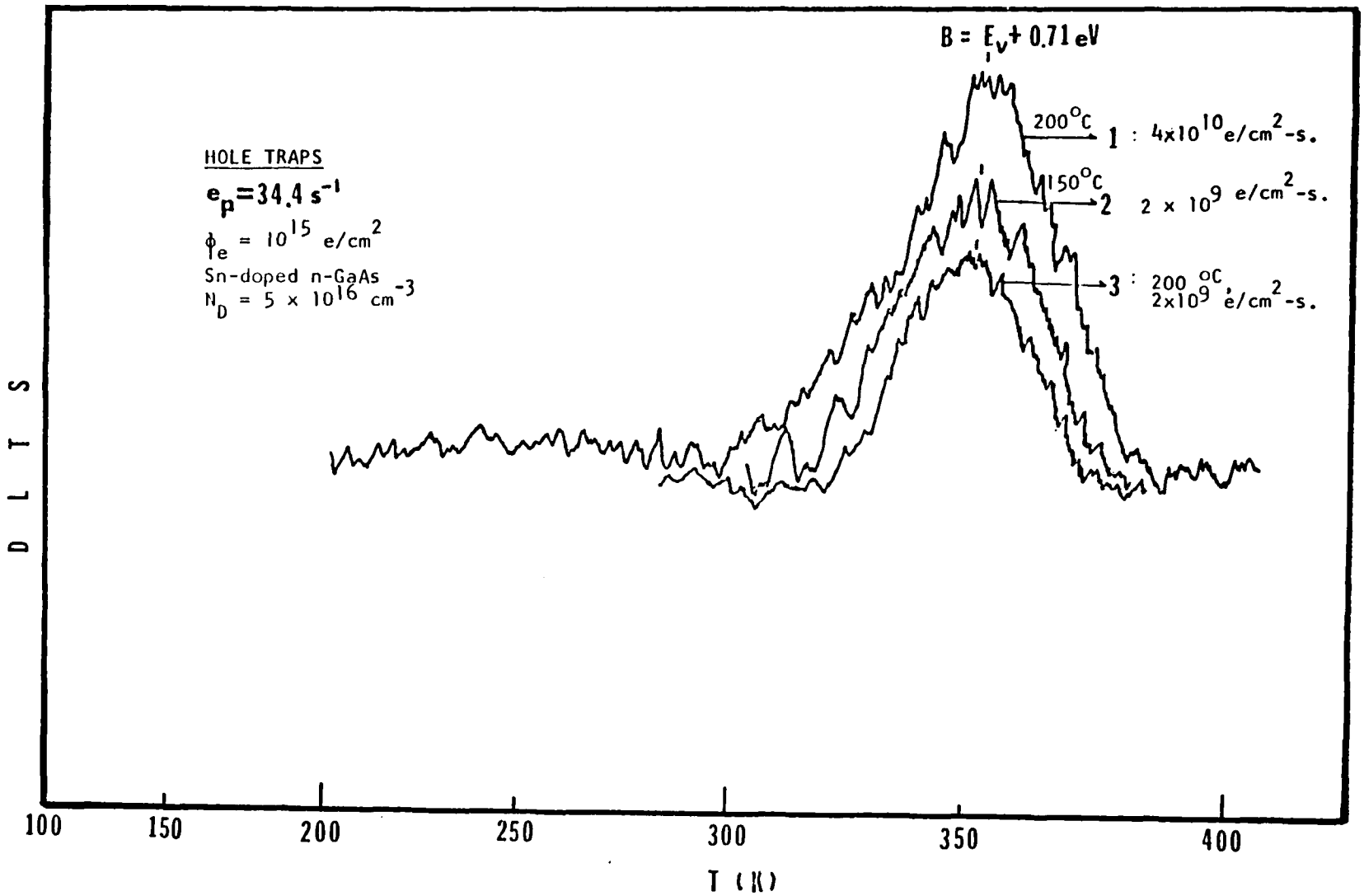

Fig. 5.10 DLTS scan of hole traps in one-MeV electron irradiated (AlGa)As-GaAs mesa diodes vs incident electron flux rate and annealing temperature.

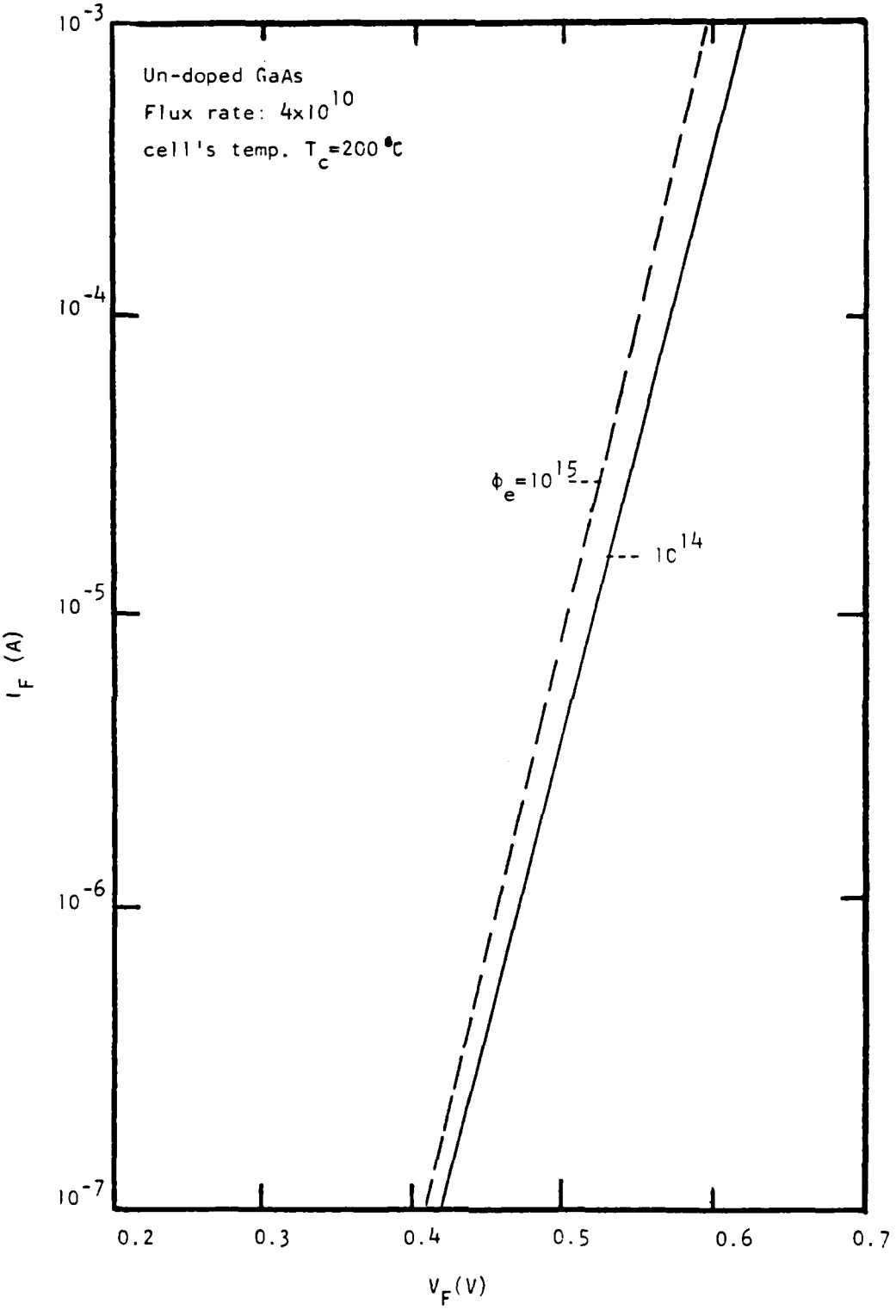

Fig. 5.11 Forward I-V characteristics for one-MeV electron irradiated (AlGa)As-GaAs mesa diodes for two electron fluences.

Table 5.3 Electron Trap Parameters vs. Flux Rate in one-MeV Electron Irradiated (AlGa) As-GaAs diodes for $\phi_e = 10^{15}$ e/cm^2

Samples	N_D (cm^{-3})	Flux Rate (e/cm^2-s)	Annealing Temp. (°C)	Electron Traps			
				E_T (eV)	N_T (cm^{-3})	σ_n (cm^{-2})	τ_n (s)*
1	5.35×10^{16}	4×10^{10}	200	$E_3=E_c-0.31$ $E_4=E_c-0.71$ $E_5=E_c-0.90$	1.24×10^{13} 5.84×10^{13} 1.35×10^{13}	1.8×10^{-14} 5.1×10^{-14} 5.8×10^{-14}	1×10^{-7} 6.85×10^{-9} 2.6×10^{-8}
2	5.56×10^{16}	2.10^{9}	150	E_4	4.85×10^{13}	5.1×10^{-14}	8.25×10^{-9}
3	5.69×10^{16}	2×10^{9}	200	E_4	3.61×10^{13}	5.1×10^{-14}	1.11×10^{-8}

Table 5.4 Hole Trap Parameters vs. Flux Rate in one-MeV Electron Irradiated (AlGa) As-GaAs diodes for $\phi_e = 10^{15}$ e/cm^2

Samples	N_D (cm^{-3})	Flux Rate (e/cm^2-S)	Annealing Temp. (°C)	Hole Traps				
				E_T (eV)	N_T (cm^{-3})	σ_p (cm^2)	τ_p (s)*	L_p (μm)*
1	5.35×10^{16}	4×10^{10}	200	EB=E_v+0.71	4.94×10^{13}	4.0×10^{-13}	3.6×10^{-9}	2.01
2	5.56×10^{16}	2×10^{9}	150	E_v+0.71	4.02×10^{13}	4.2×10^{-13}	4.46×10^{-9}	2.23
3	5.69×10^{16}	2×10^{9}	200	E_v+0.71	3.06×10^{13}	4.0×10^{-13}	5.84×10^{-9}	2.58

*$\tau_p = (N_T \sigma_p V_{th})^{-1}$, $L_p = (\tau_p D_p)^{1/2}$; $D_p = 11.2$ cm^2/s.

increasing electron fluence. This result is directly related to the deep level defects induced by the electron irradiation in the GaAs, as is evidenced by the DLTS results. Fig.5. 12 shows the DLTS scans of electron traps for GaAs irradiated with 1xE14 and 1xE15 e/cm2 fluence and continueously annealed at 200 C; four electron traps with energies of Ec-0.13, 0.41, 0.71, and 0.90 eV were observed in these samples. Note that Ec-0.13 and Ec-0.41 eV electron traps were not detected in the Sn-doped GaAs shown in Fig.5. 3, while Ec-0.31 eV electron trap observed in the Sn-doped GaAs was not detected in the undoped GaAs. Another interesting result for the undoped GaAs is that the dominant electron traps are due to the Ec-0.13 and 0.41 levels, with trap density one to two orders of magnitude higher than that of Ec-0.71 and 0.90 eV electron traps. The DLTS scan of hole traps for the undoped GaAs is shown in Fig.5.13 for two electron fluences. Two hole traps with energies of Ev+0.29 and 0.71 eV were observed in GaAs irradiated with 1xE15 e/cm2 fluence, and only one hole trap with energy of Ev+0.71 eV was observed in diode irradiated with 1xE14 e/cm2 fluence. Note that both electron and hole trap density was found to increase with increasing electron fluence; the Ev+0.29 eV hole trap observed in the undoped GaAs was not detected in the Sn-doped GaAs. Table.5.5 summarizes the defect and recombination parameters deduced from the DLTS and C-V data for the undoped GaAs shown in Fig.5.12 and Fig.5. 13. In addition to the low temperature thermal annealing study discussed above, we have also conducted a combined thermal and recombination enhanced (by applying a forward bias current to the

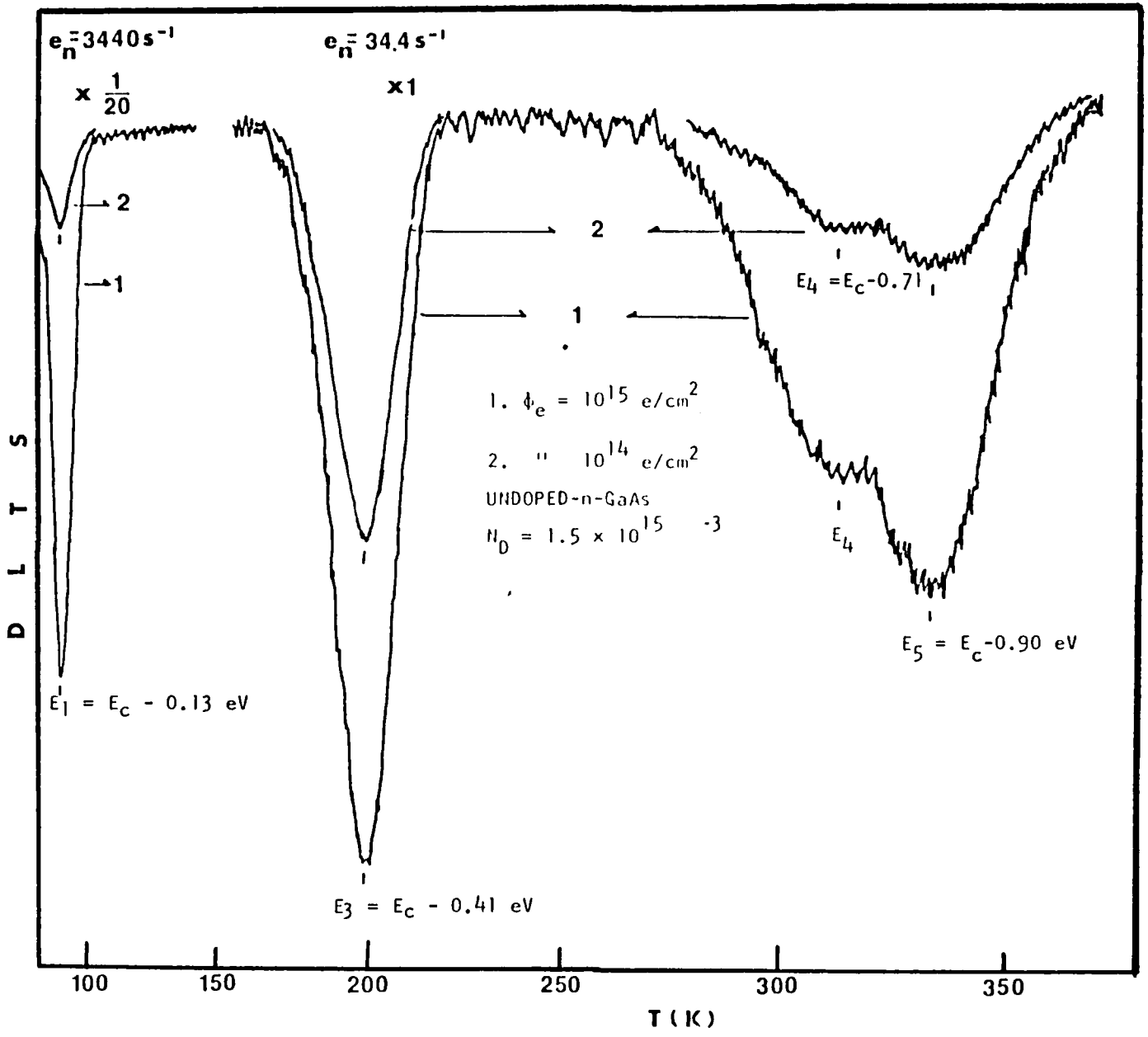

Fig. 5.12 DLTS scan of electron traps in one-MeV electron irradiated (at 200 °C) (AlGa)As-GaAs mesa diodes as a function of electron fluence

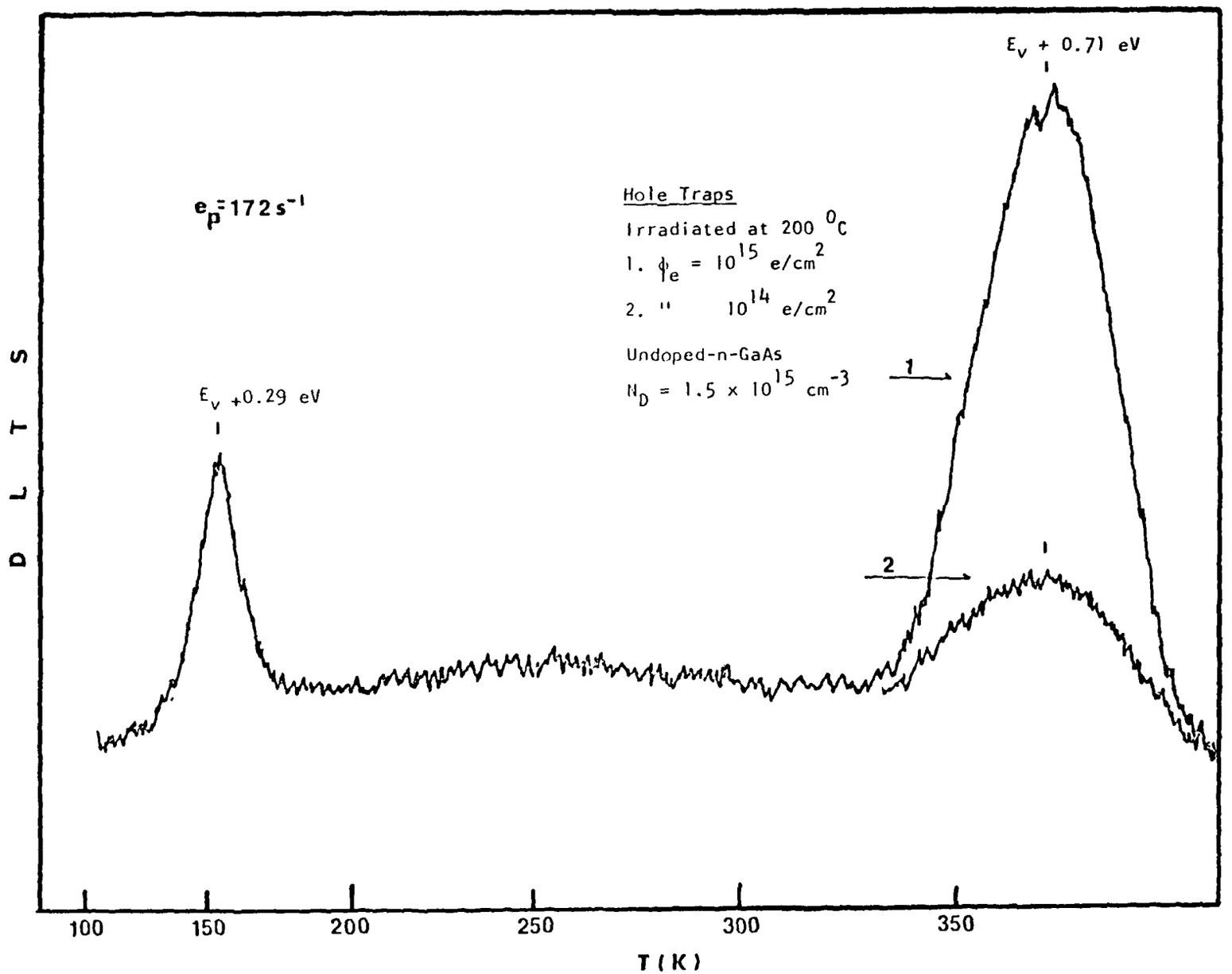

Fig. 5.13 DLTS scan of hole traps in one-MeV electron irradiated (at 200 °C) (AlGa)As-GaAs mesa diodes as a function of electron fluence.

Table 5. 5 Defect parameters of Hole Traps in one-MeV Electron Irradiated (AlGa) As-GsAs diodes vs. Annealing Time

Fluence (e/cm^2)	N_D (cm^{-3})	Annealing Time & Temp.	Hole Traps				
			E_T (eV)	N_T (cm^{-3})	σ_p (cm^2)	τ_p (ns)	L_p (μm)
10^{15}	5.5×10^{16}	20 min. at 230°C	E_v+0.71	9×10^{13}	4.01×10^{-13}	2.25	1.50
		30 " "	"	6.8×10^{13}	"	2.65	1.72
		60 " "	"	3.4×10^{13}	"	5.30	2.44
10^{16}	3.5×10^{16}	20 min. at 230°C	E_v+0.71	9×10^{14}	4.01×10^{-13}	0.20	0.47
		30 " "	"	6.2×10^{14}	"	0.29	0.57
		60 " "	"	1.1×10^{14}	"	1.64	1.35

diode) annealing study on some of the undoped GaAs irradiated by one-MeV electrons at 200 C. Fig.5.14 through Fig.5.16 showed the DLTS results for the electron and hole traps observed in these diodes with and without recombination-enhanced annealing (REA) process. Fig.5.14 shows the DLTS scans of electron traps before and after four cycles of REA process for 1xE15 e/cm2 fluence. Note that the REA process is very effective in further reducing the density of each electron trap induced by one-MeV electron irradiation. Fig.5.15 shows the DLTS scans of electron traps before and after four cycles of the REA process for 1xE14 e/cm2 fluence. The results again showed a significant reduction in the density of each electron trap by the REA process. Fig.5.16 shows the DLTS scan of hole traps before and after REA process for electron fluence of 1xE15 e/cm2. The hole trap density was significantly reduced after four cycles of REA process. The REA process was particularly effectve for reducing the density of deeper hole trap (i.e. Ev+0.71 eV). Thus, it is obvious that a combined low temperature thermal and recombination enhanced annealing process is a powerful technique to eliminate the one - MeV electron radiation induced defects in the GaAs LPE layers.

5.5 Undoped GaAs Irradiated at 27°C with Electron Fluences of 1xE14 to 1xE16 e/cm2

Study of deep-level defects in the undoped GaAs irradiated at room temperature for four different electron fluences has also been carried out in this work, and the results are discussed next. Fig.5.17 shows the thermally stimulated capacitance (TSCAP) scans for the undoped GaAs irradiated with electron fluences of

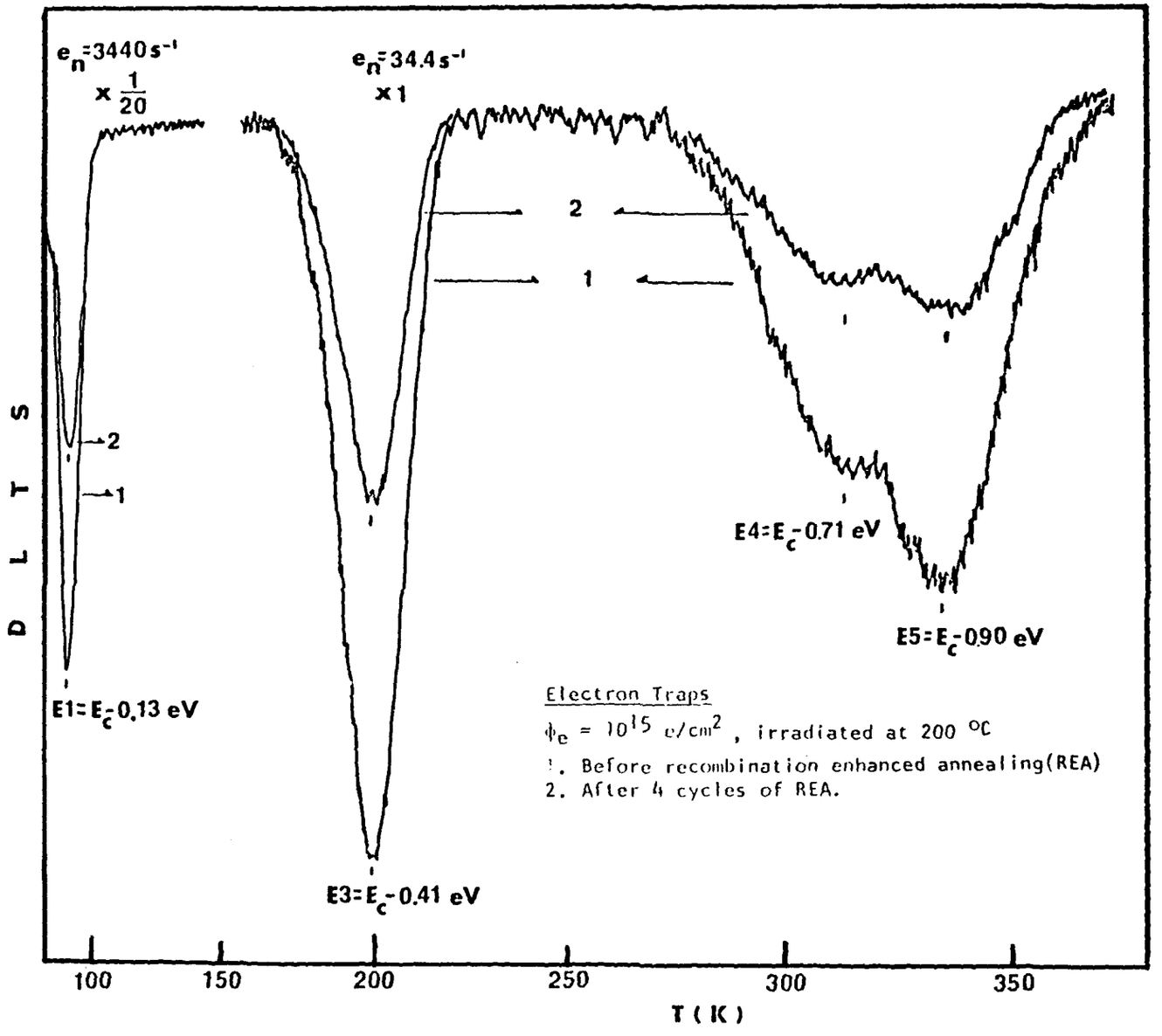

Fig. 5.14 DLTS scan of electron traps in one-MeV electron irradiated (AlGaAs)-GaAs mesa diodes with and without recombination enhanced annealing.

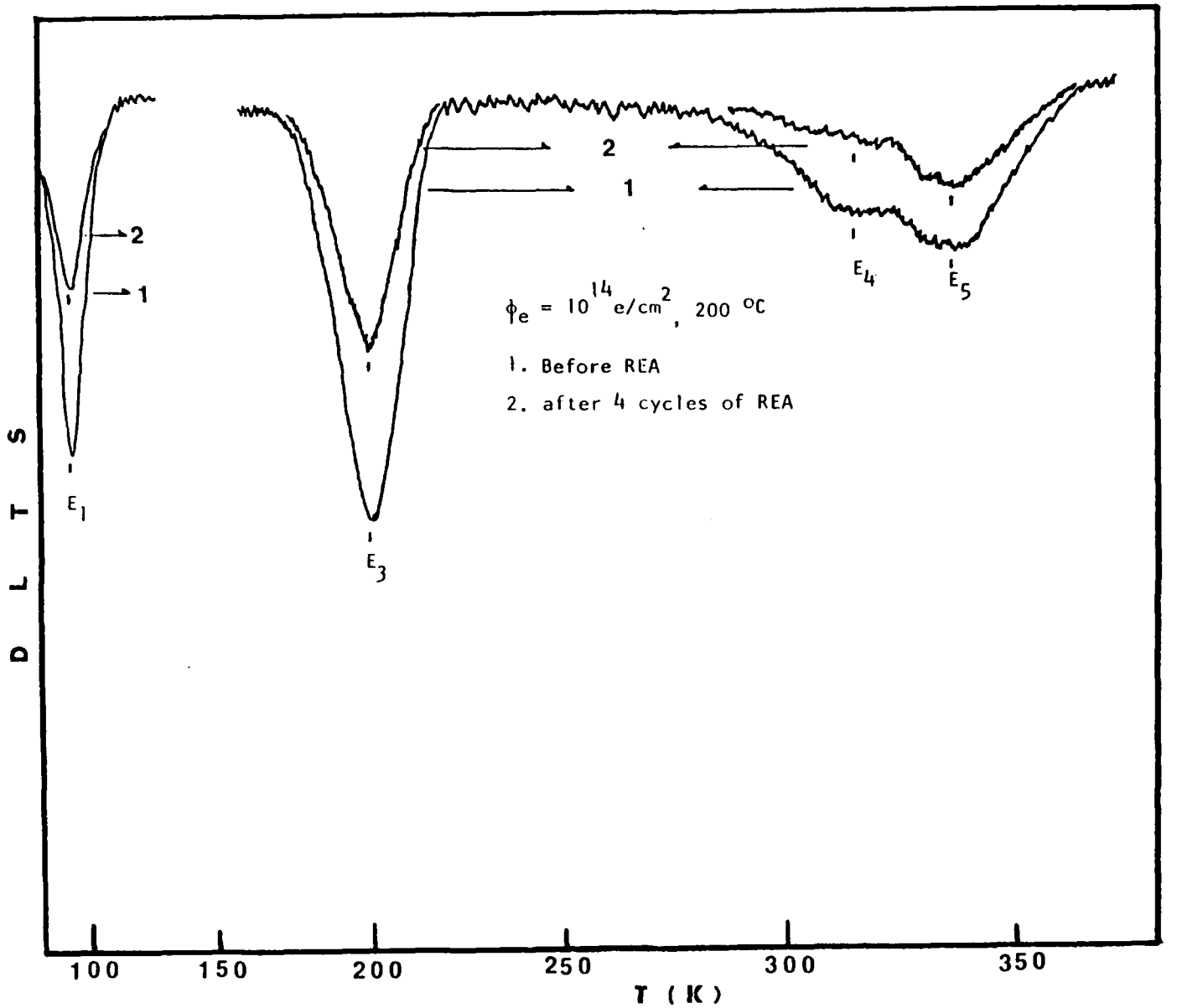

Fig. 5.15 DLTS scan of electron traps in one-MeV electron irradiated (AlGa)As-GaAs mesa diodes with and without recombination enhanced annealing(REA).

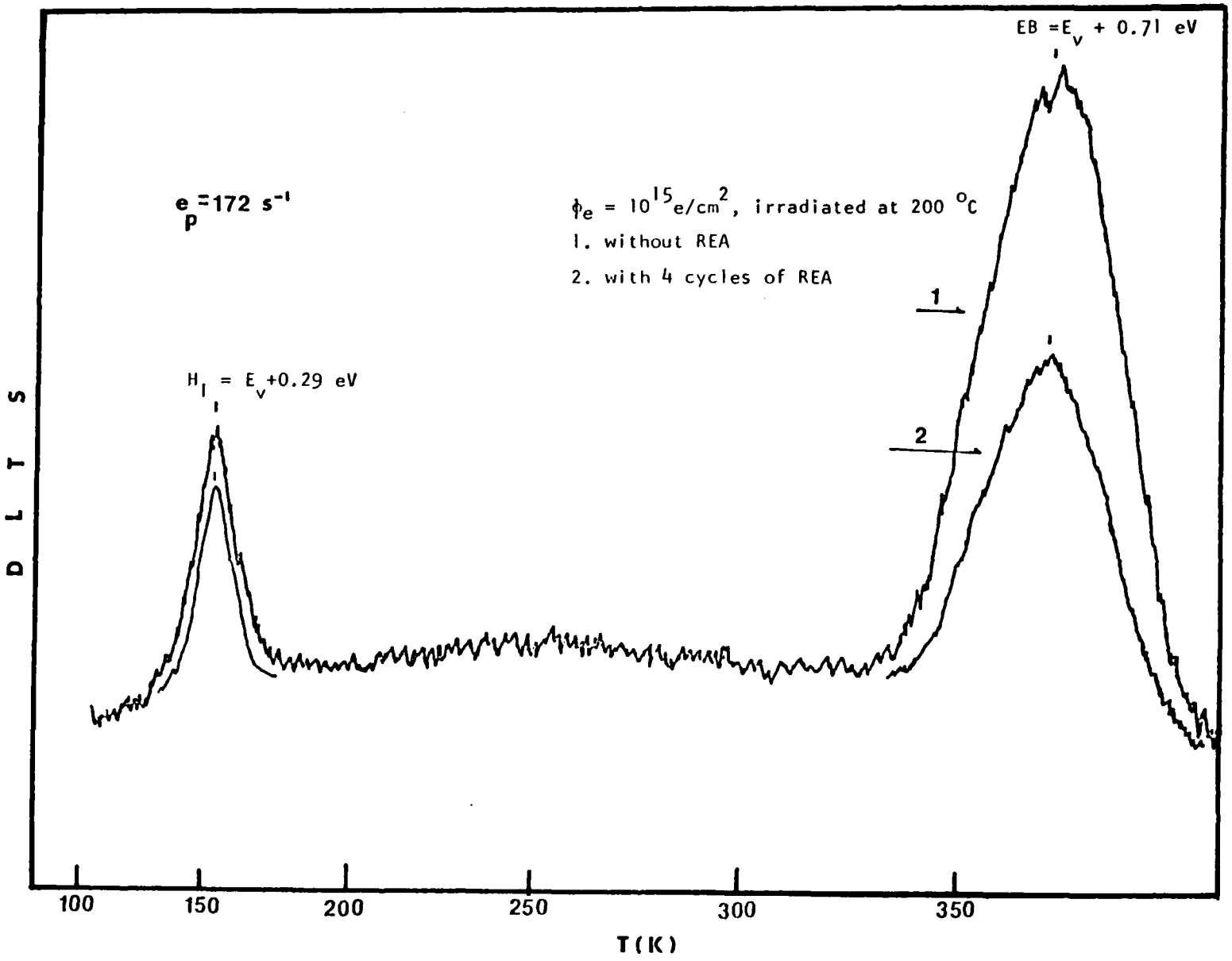

Fig. 5.16 DLTS scan of hole traps in the one-MeV electron irradiated (AlGaAs)-GaAs mesa diodes with and without recombination enhanced annealing (REA).

1xE14, 1xE15, 5xE15, and 1xE16 e/cm2. The results showed that for 1xE14 e/cm2 electron fluence, the capacitance curve showed no features of deep-level defects, and the capacitance was increased gradually with increasing temperature. However, at 1xE15 and 5xE15 e/cm2 electron fluences, there were significant changes in the capacitance value for temperatures between 100 and 160 K. The main reason for this capacitance change is due to the electron emission from the E3 electron trap, as can be shown in the DLTS data. For 1xE16 e/cm2 electron fluence, no change in the capacitance was detected in the temperature range between 77 and 200 K, instead a capacitance step was observed between 250 and 300 K. This result can be explained by the fact that at low temperature, the density of H1 (Ev+0.29 eV) hole acceptor level is nearly equal to the background carrier density, and as a result of compensation an insulating layer was created in the n-GaAs layer of for temperature below 200 K where capacitance value remains constant. In fact the temperature dependance of the TSCAP shown in Fig.5.17 can be best interpreted with the help of DLTS data shown in Fig.5.19 through Fig.5. 26 for the undoped GaAs irradiated by four different electron fluence. Fig.5.18 shows the capacitance vs reverse bias voltage for the undoped GaAs as a function of electron fluence. The results showed that capacitance value was decreased with increasing electron fluence, indicating carrier removal occured in the samples as a result of one-MeV electron irradiation; the carrier removal rate was found to be equal to 0.3 /cm. The DLTS scans of electron traps as a function of electron fluence are shown in Fig.5.19 through Fig.5.22 for

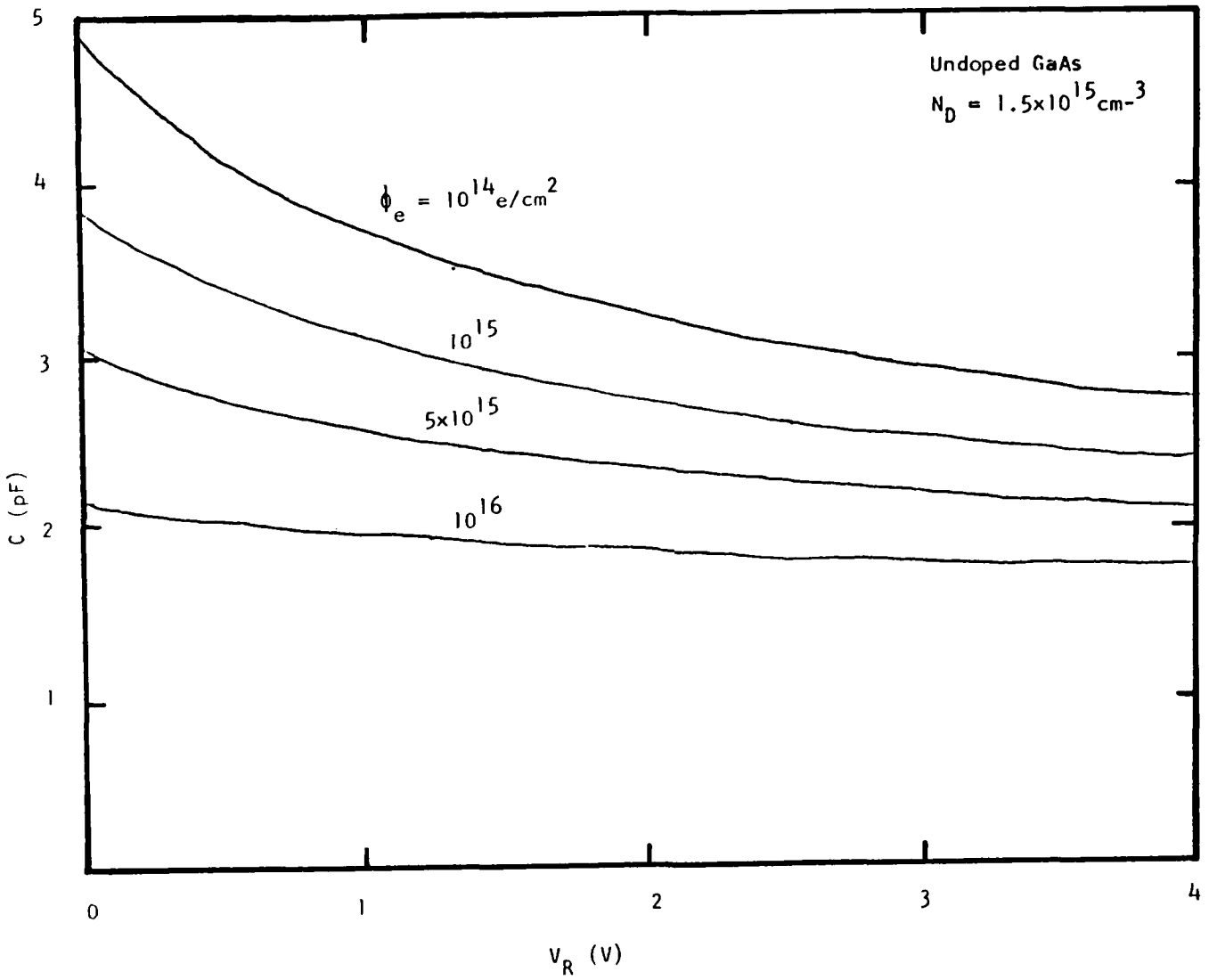

Fig. 5.18 Capacitance of one-MeV electron-irradiated (AlGa)As-GaAs mesa diodes vs reverse bias for different electron fluences.

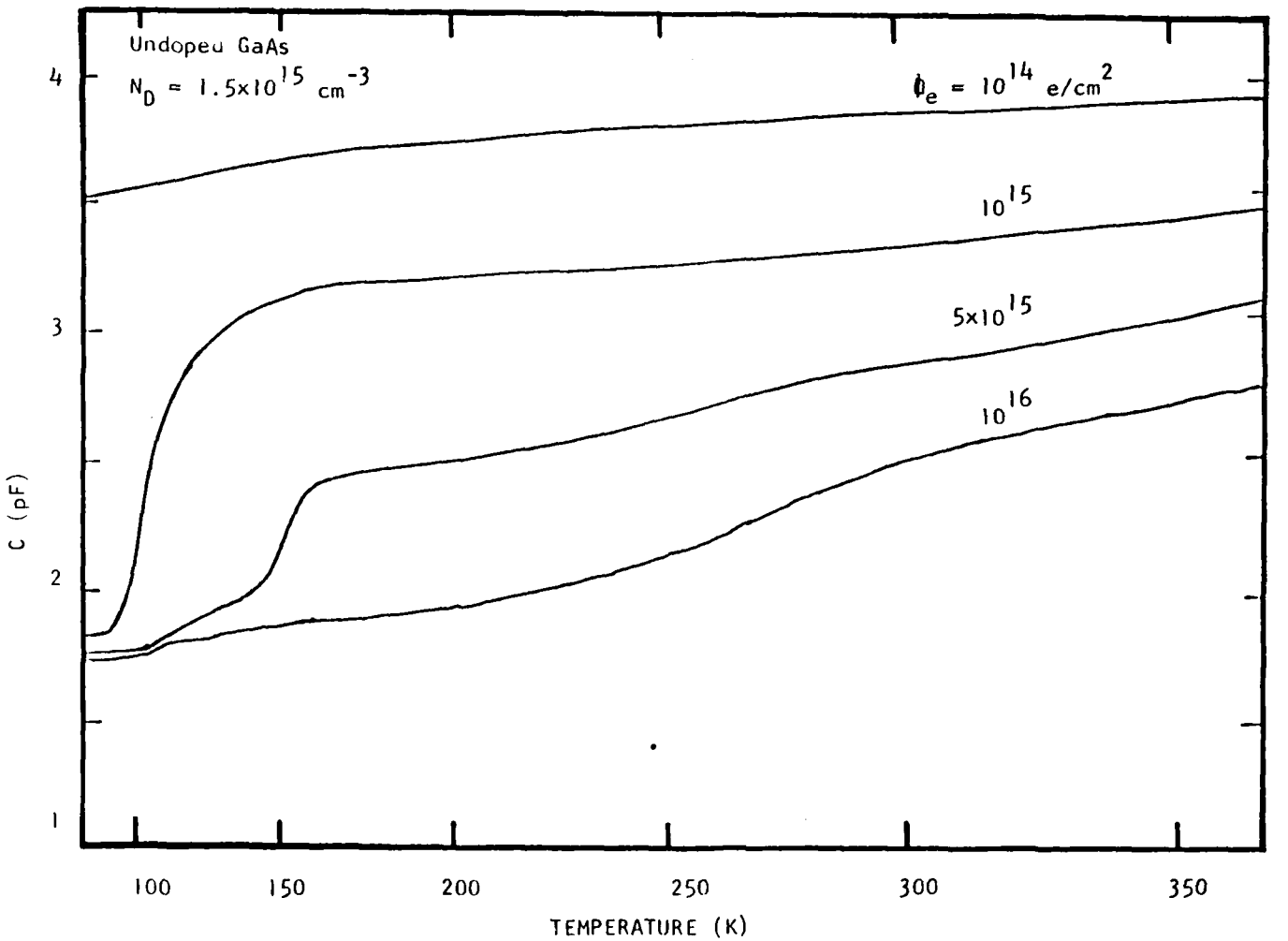

Fig. 5.17 Capacitance of one-MeV electron-irradiated (AlGa)As-GaAs mesa diodes vs temperature for different electron fluences.

electron fluences of 1xE14, 1xE15, 5xE15, and 1xE16 e/cm2, respectively. The results clearly showed that the density and number of electron traps were increased with increasing electron fluence. For 1xE14 e/cm2 fluence, only two shallow electron traps with energies of E1 = Ec-0.13 and E3 = Ec-0.41 eV were observed in the sample. As electron fluence increases to 1xE15 e/cm2, the E3 electron trap becomes the dominant trap, while deeper levels such as E4 = Ec-0.71 and E5 = Ec-0.90 eV starting to appear in the DLTS scan; this becomes more clear at 5xE15 e/cm2 electron fluence. At 1xE16 e/cm2 electron fluence, the dominant electron traps are due to E3, E4, and E5 levels, as is shown in Fig.5.22. The DLTS scans for the hole traps in these undoped GaAs LPE layers as a function of electron fluence are shown in Fig. 5.23 through Fig.5.26, respectively. For 1xE14 e/cm2 electron fluence, only one hole trap was detected in the sample with energy of HB = Ev +0.71 eV. As fluence increases to 1xE15 e/cm2, three additional hole traps with energies of H0 = Ev + 0.20 eV, H1 = Ev + 0.29 eV, and H2 = Ev + 0.35 eV were observed in this sample. These hole trap levels continue to grow with increasing electron fluence as is evidenced by the DLTS scans shown in Fig.5.25 for fluence of 5xE15 and in Fig.5.26 for fluence of 1xE16 e/cm2. Note that at 1xE16 e/cm2 fluence, another hole trap with energy of H3 = Ev + 0.40 eV was detected. Thus, at 1xE16 e/cm2 electron fluence, there are five hole traps and three electron traps observed in the one-MeV electron irradiated GaAs sample. The density of shallow hole traps such as H1 and H2 levels is quite large for 1xE16 e/cm2 electron fluence, and is comparable to the background carrier density in the n-GaAs

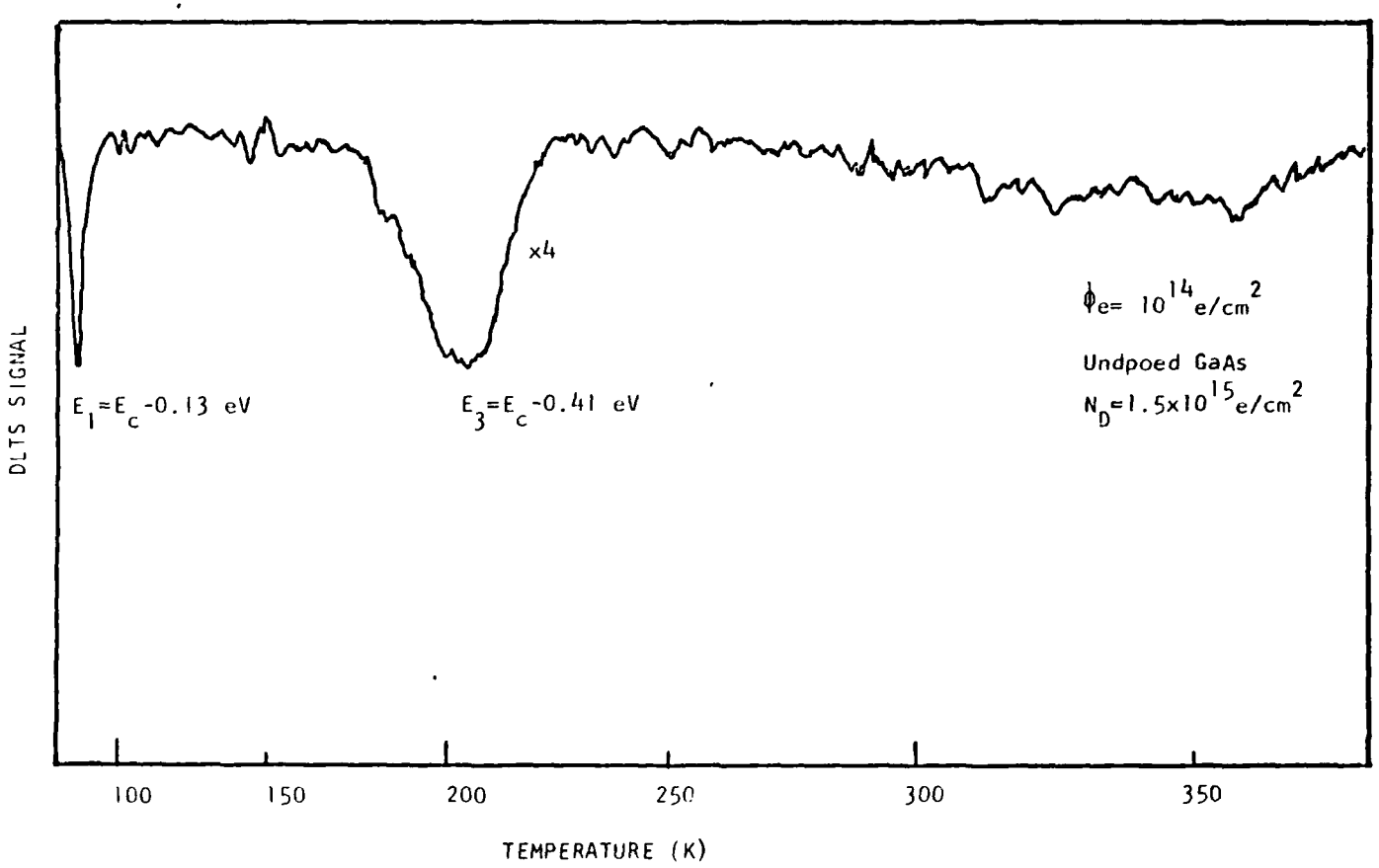

Fig. 5.19 DLTS scan of electron traps for one-MeV electron irradiated (AlGa)As-GaAs mesa diodes with electron fluence of 10^{14} e/cm^2.

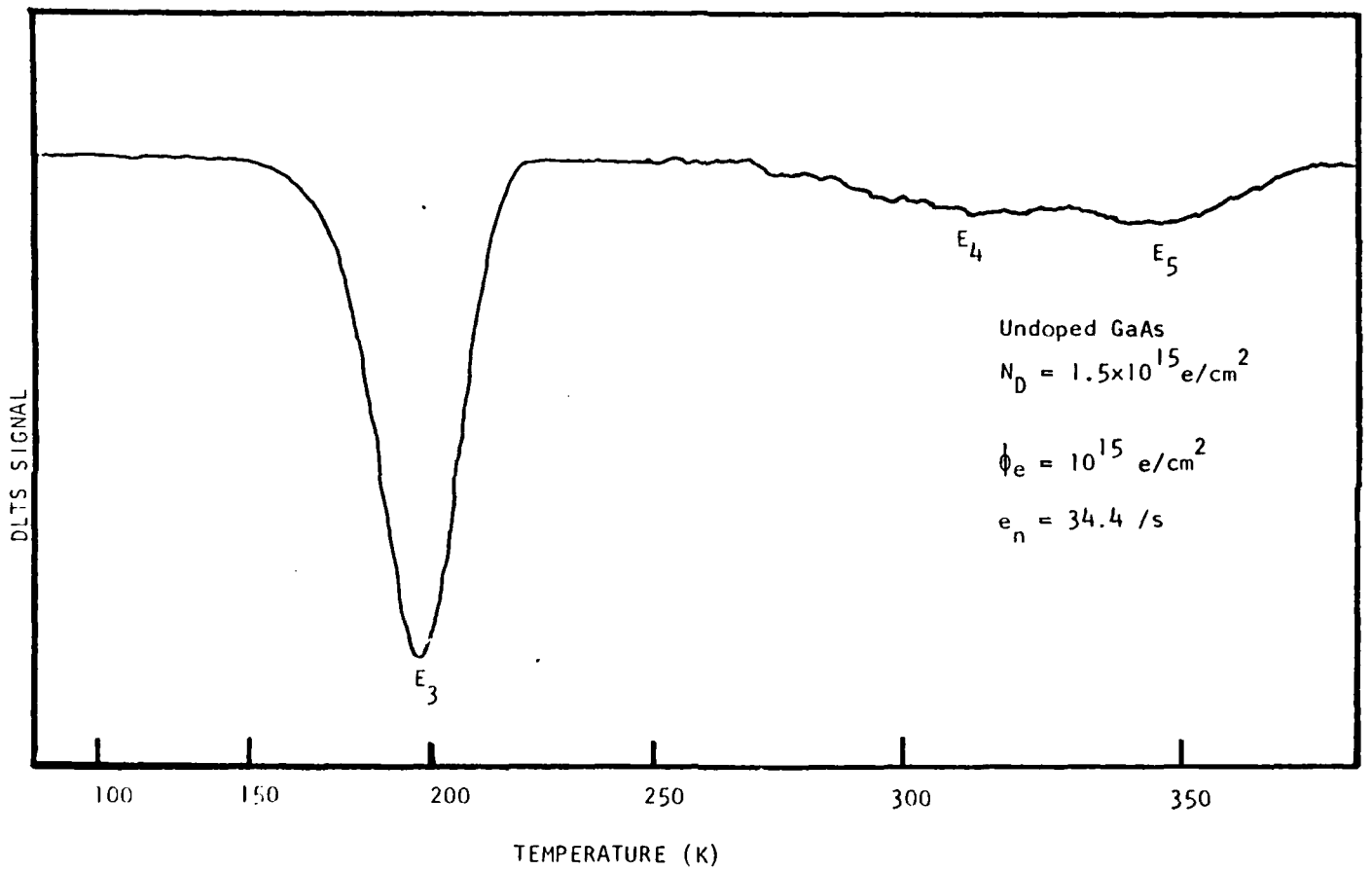

Fig. 5.20 DLTS scan of electron traps for one-MeV electron irradiated (AlGa)As-GaAs diodes with 10^{15} e/cm^2 fluence.

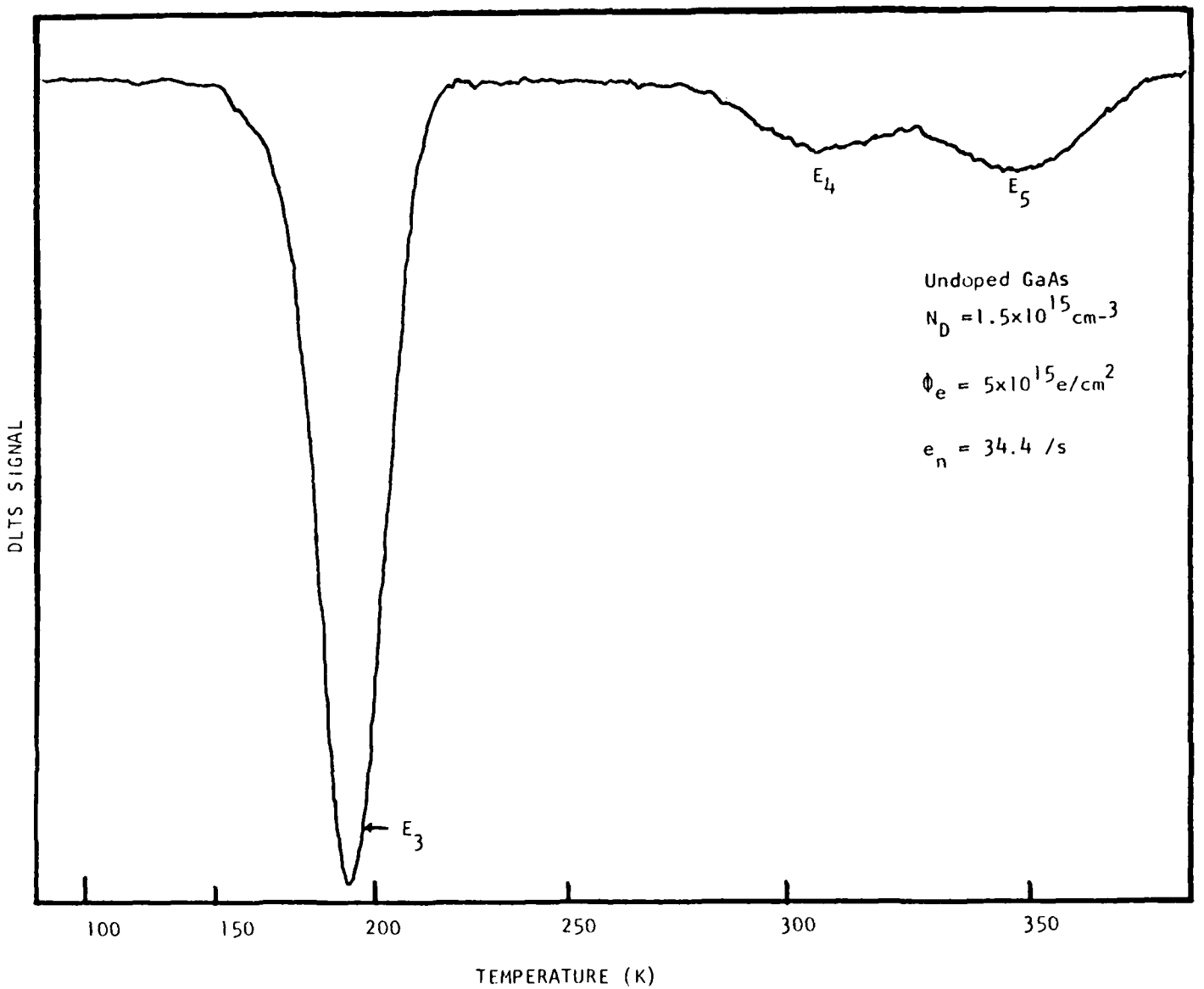

Fig. 5.21 DLTS scan of electron traps in one-MeV electron irradiated (AlGa)As-GaAs diodes for electron fluence of 5×10^{15} e/cm^2.

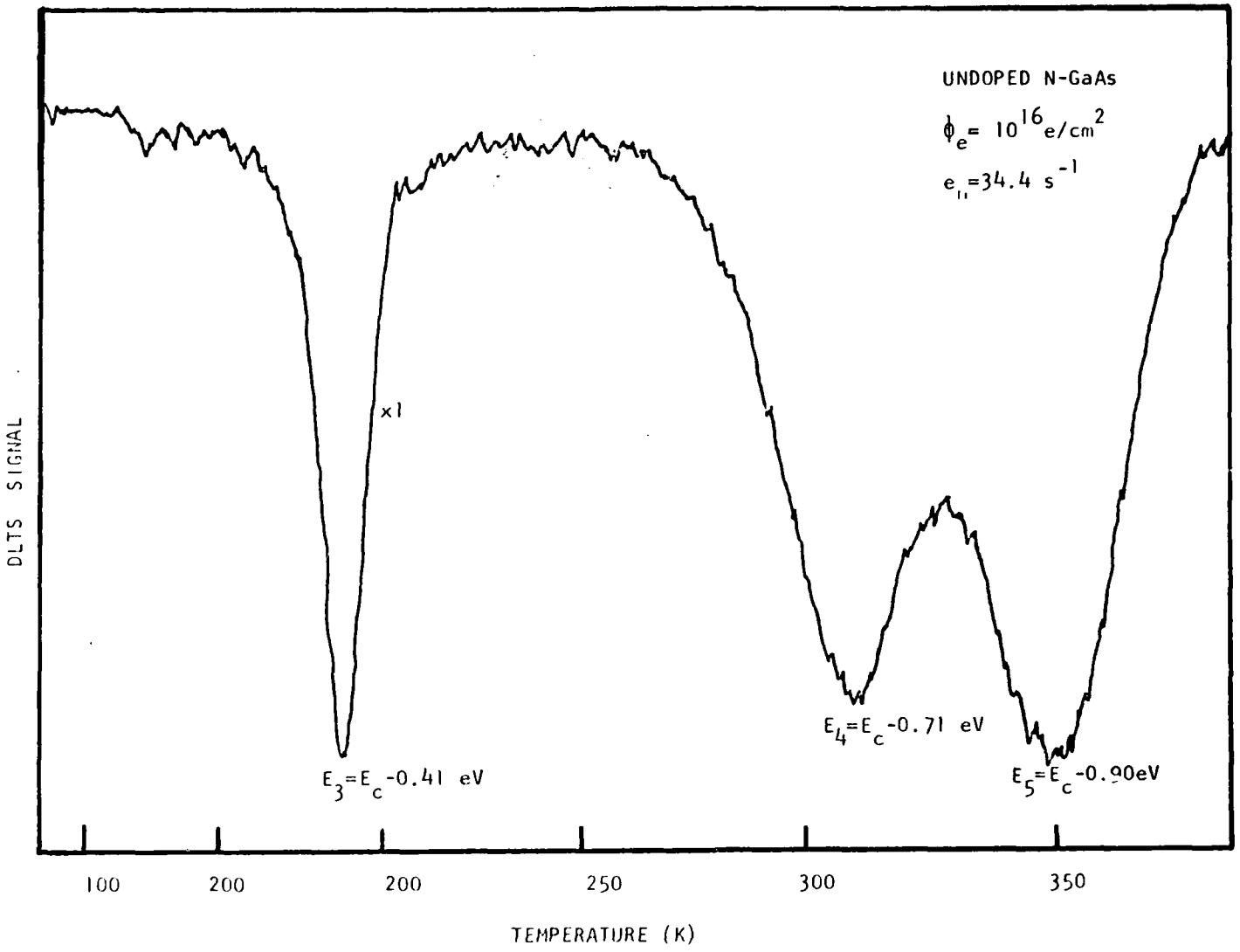

Fig. 5.22 DLTS scan of electron traps in one-MeV electron irradiated (AlGa)As-GaAs diodes for 10^{16} e/cm^2 electron fluence.

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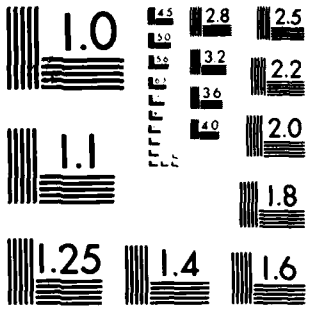

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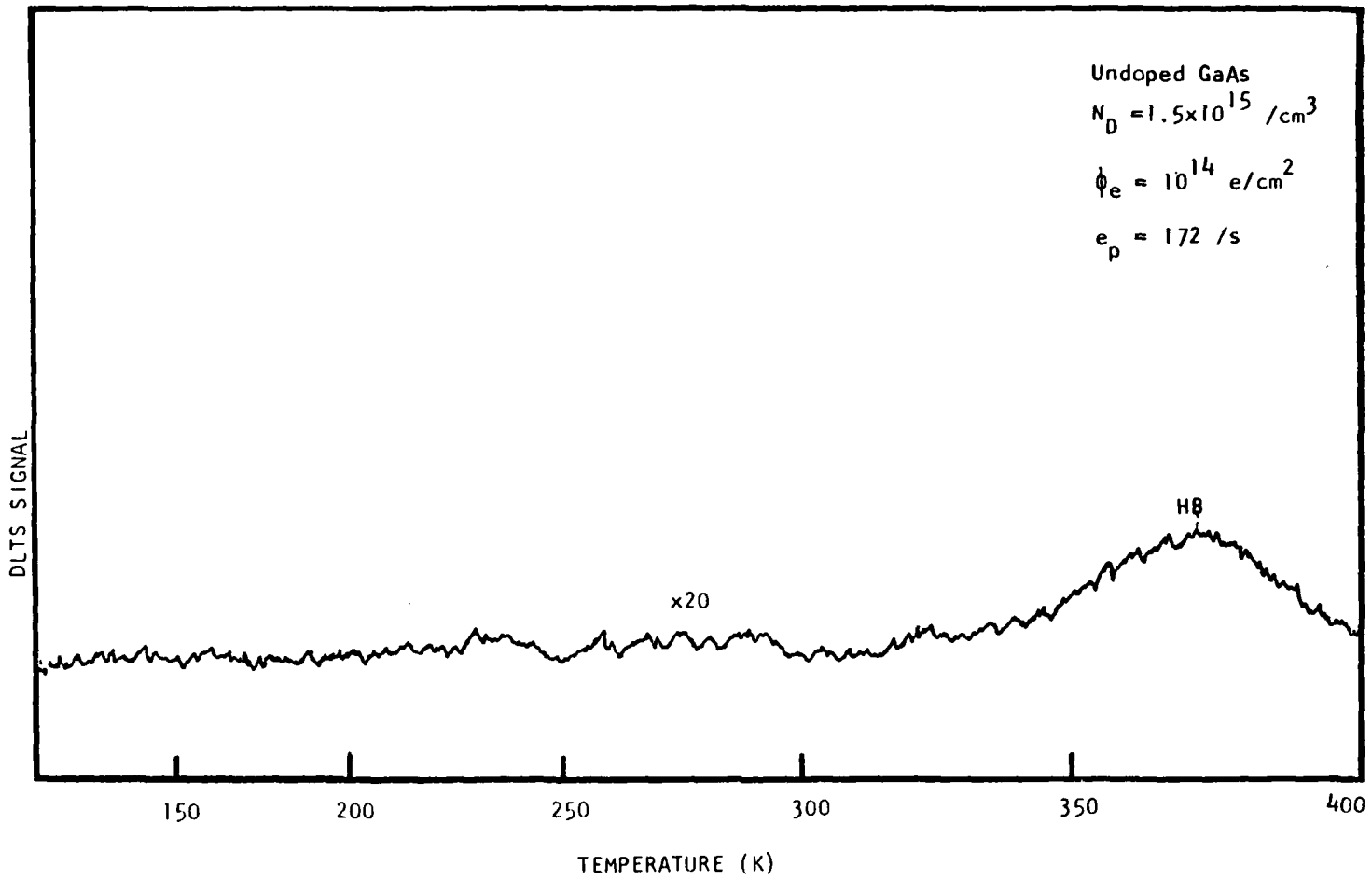

Fig. 5-23 DLTS scan of hole traps in one-MeV electron irradiated (AlGa)As-GaAs mesa diodes for 10^{14} e/cm^2 electron fluence.

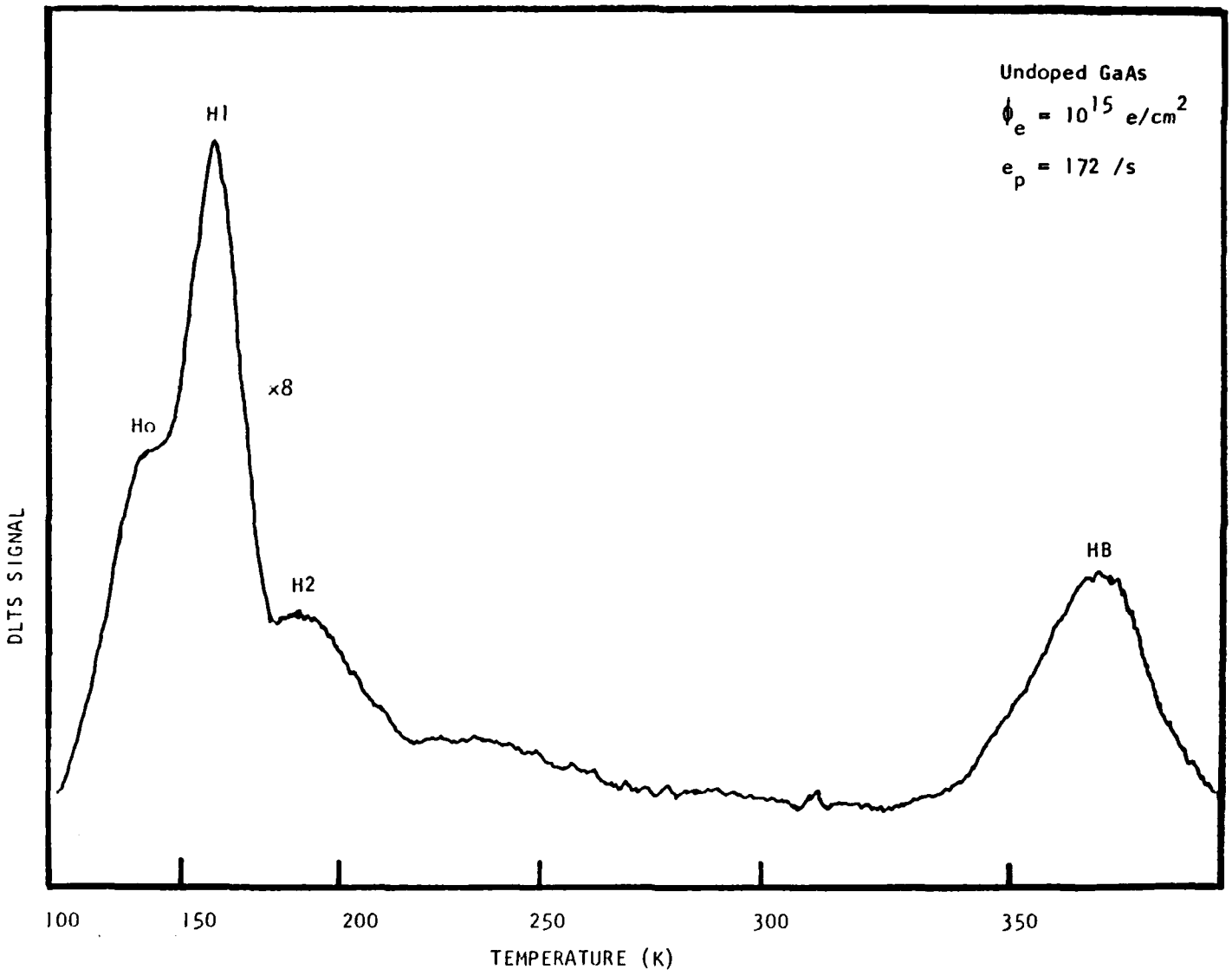

Fig. 5.24 DLTS scan of hole traps in one-MeV electron irradiated (AlGa)As-GaAs mesa diode.

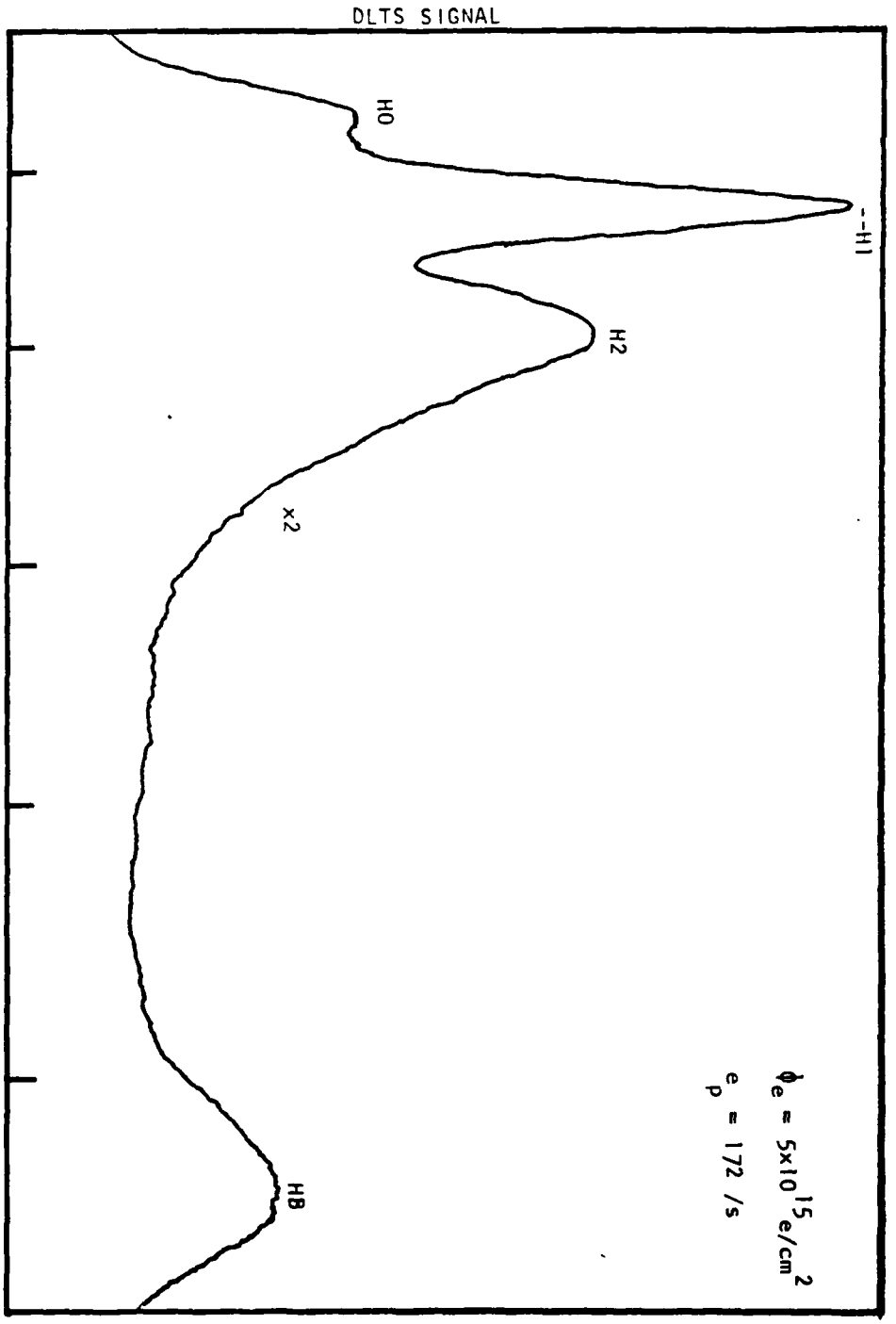

Fig. 5.25 DLTS scan of hole traps in one-MeV electron irradiated (AlGa)As-GaAs mesa diode.

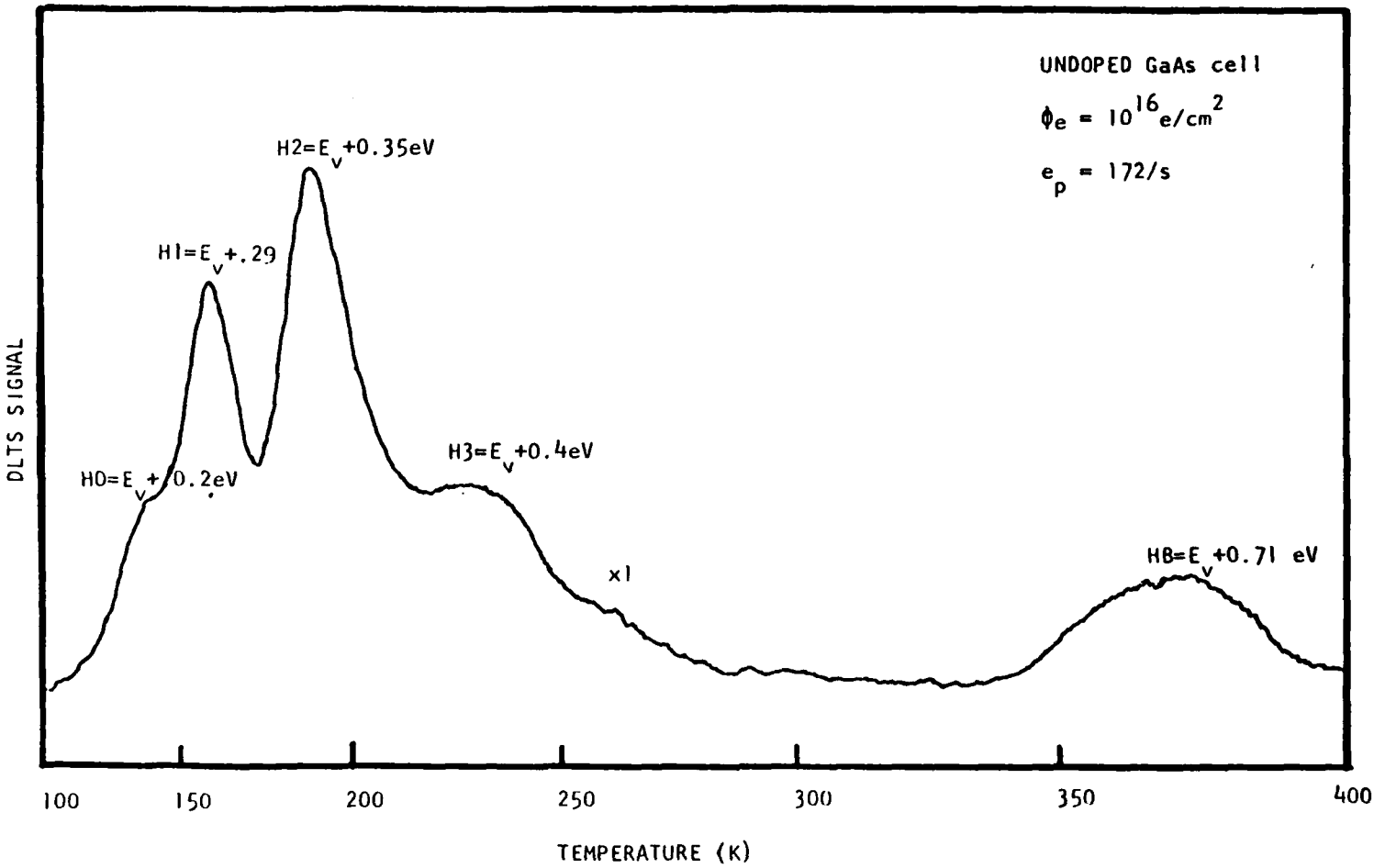

Fig.5.26 DLTS scans of hole traps in one-MeV electron-irradiated (AlGa)As-GaAs mesa diode.

active layer. Note that the deep level traps such as E4, E5, and HB are the dominant recombination centers in these electron irradiated GaAs, and the defect parameters deduced from the DLTS data can be used to calculate the recombination parameters such as lifetimes and diffusion lengths in the samples. Table.5. 6 summarizes the defect and recombination parameters deduced from the DLTS data for the one-MeV electron irradiated GaAs samples for four different electron fluences. The carrier removal rate and the defect density vs electron fluence for the undoped GaAs irradiated at room temperature for four different fluences are shown in Fig.5. 27 and Fig.5. 28, respectively. Fig.5.27 shows the carrier density and the density of electron traps (E3, E4,and E5) vs electron fluence for these samples. Fig. 5.28 shows the density of hole traps (H1, H2, H3, and HB) vs electron fluence for the undoped GaAs discussed above. It is interesting to note that density of both electron and hole traps increases rapidly with increasing electron fluence initially, and becomes saturated at 1xE16 e/cm2 fluence when the defect density is comparable to the background density in the undoped n-GaAs layer.

A comparison of the DLTS results for the undoped GaAs irradiated at 200 C and at room temperature reveals that several shallow hole traps such as Ho, H1, H2, and H3 which were observed in the room temperature irradiated GaAs were not detected in the 200 C annealed samples. This suggested that these hole traps were completely annealed out by raising the specimen temperature to 200 C during electron irradiation. No significant difference was observed in the DLTS spectrum for the electron traps in both cases.

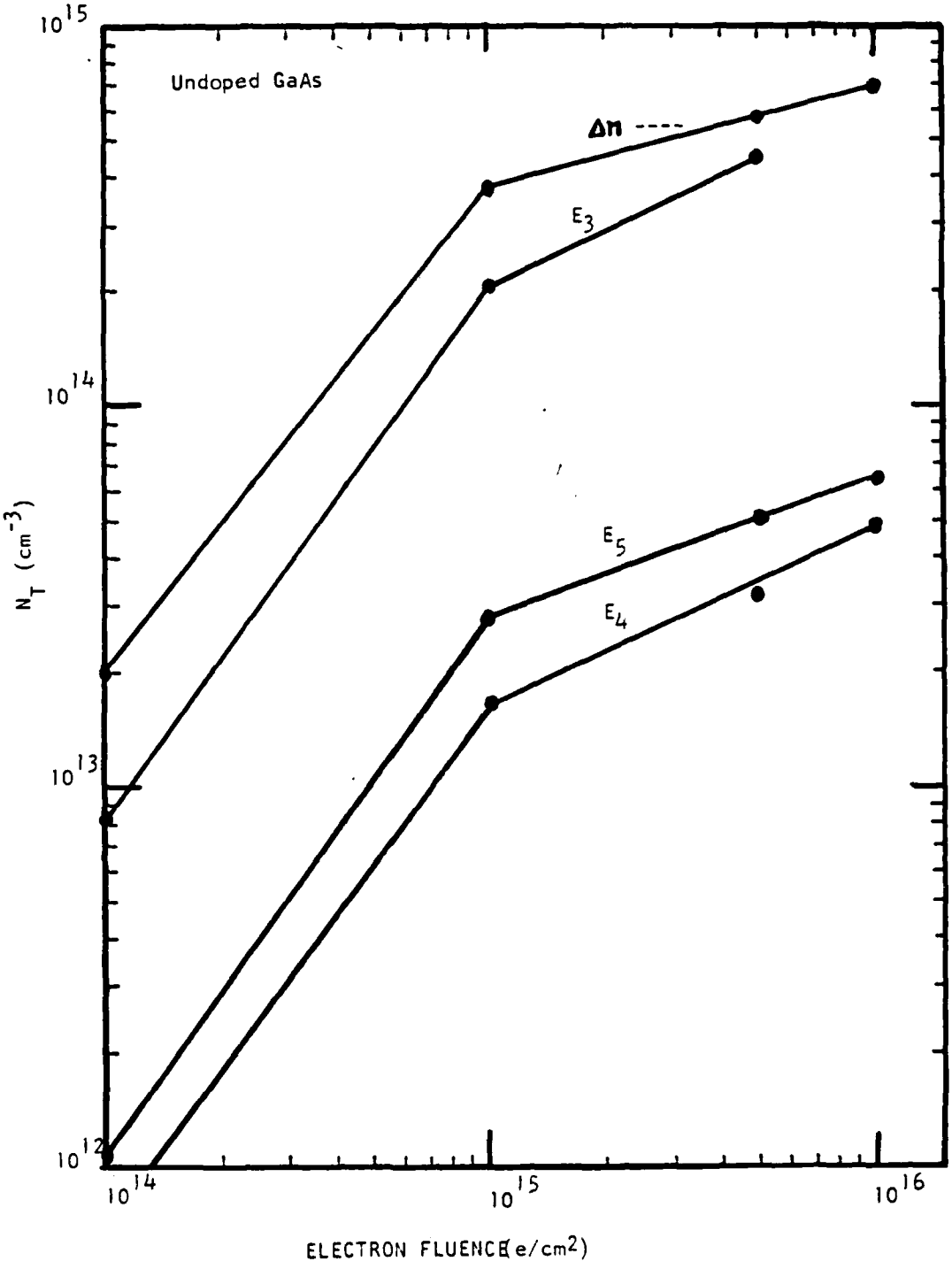

Fig. 5.27 Defect density and free carrier density vs electron fluence in one-MeV electron irradiated (AlGa)As-GaAsmesa diode .

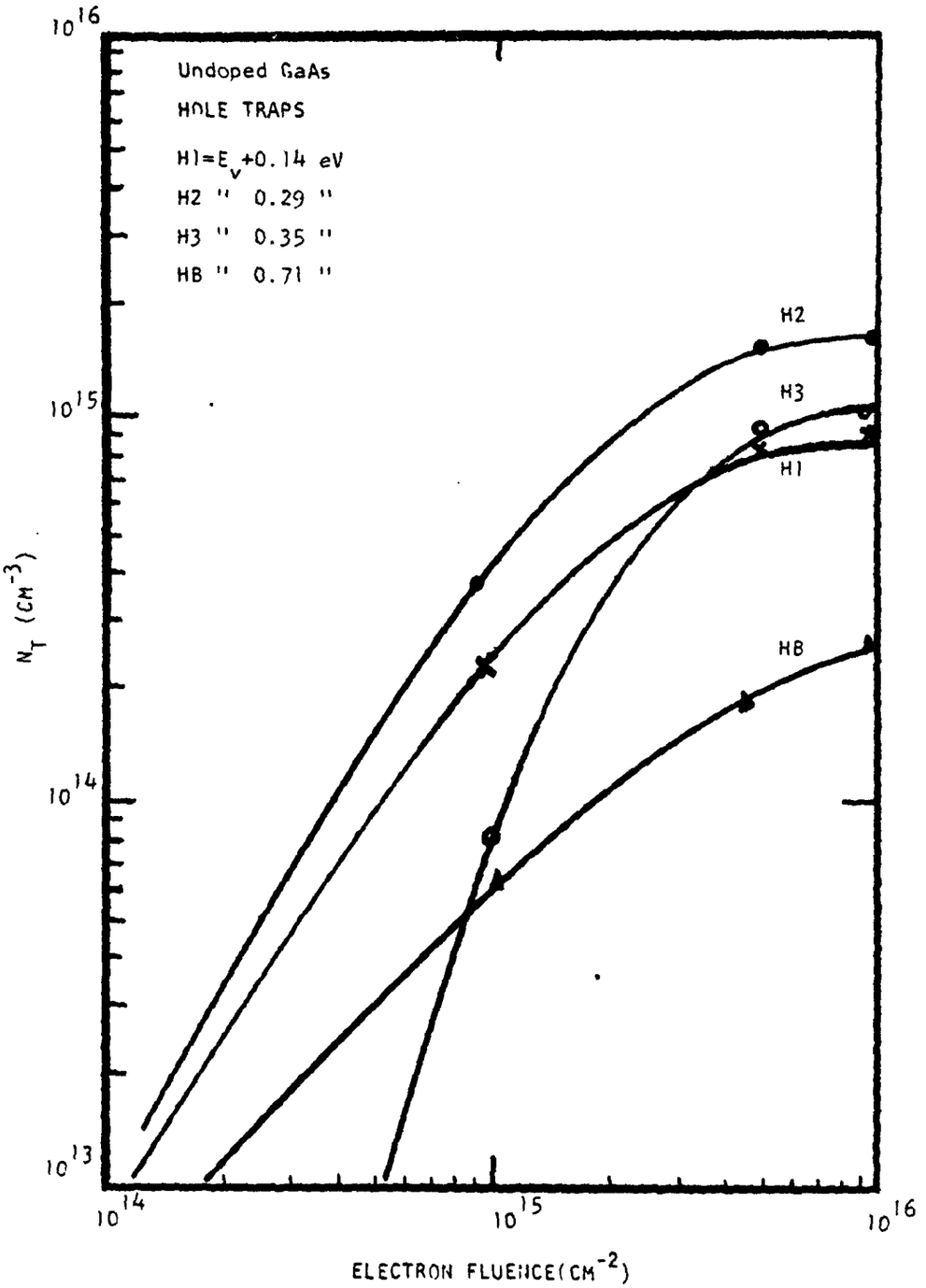

Fig. 5. 28 Density of hole traps vs electron fluence in one-MeV electron-irradiated (AlGa)As-GaAs mesa diode.

Table 5.6 Defect parameters in one–MeV electron irradiated (AlGa) As–GaAs diodes.*

Fluence (e/cm2)	ND (cm–3)	Electron Traps		Hole Traps	
		ET (eV)	NT (cm–3)	ET (eV)	NT (cm–3)
1 x E 14	1.5 x E 15	E1 = Ec – 0.14	1.8 x E 13	HB = Ev + 0.71	3 x E 12
		E3 = Ec – 0.41	8.2 x E 12	––	––
		E4 = Ec – 0.71	––	––	––
		E5 = Ec – 0.90	8.8 x E 11	––	––
1 x E 15	1.1 x E 15	E3 = Ec – 0.41	2.1 x E 14	H1 = Ev + 0.13	2.2 x E 14
		E4 = Ec – 0.71	1.7 x E 13	H2 = Ev + 0.29	4 x E 14
		E5 = Ec – 0.90	2.8 x E 13	H3 = Ev + 0.35	8 x E 13
				HB = Ev + 0.71	6.4 x E 13
5 x E 15	9.4 x E 14	E3 = Ec – 0.41	4.5 x E 14	H1 = Ev + 0.13	8.9 x E 14
		E4 = Ec – 0.71	3.2 x E 13	H2 = Ev + 0.29	1.5 x E 15
		E5 = Ec – 0.90	5 x E 13	H3 = Ev + 0.35	1.5 x E 15
				HB = Ev + 0.71	1.9 x E 14
1 x E 16	8.4 x E 14	E3 = Ec – 0.41	8.8 x E 13	H1 = Ev + 0.13	8.4 x E 14
		E4 = Ec – 0.71	5 x E 13	H2 = Ev + 0.29	1.6 x E 15
		E5 = Ec – 0.90	6.5 x E 13	H3 = Ev + 0.35	1 x E 15
				HB = Ev + 0.71	2.7 x E 14

* Carrier removal rate = 0.3 /cm.

VI. Summary and Conclusions

In this report, we have presented our research findings from three different research tasks: (1) Defect and transport study in LEC grown Zn-doped InP and n-InP bulk materials, (2) defect characterization in LEC grown GaAs vs annealing temperature in the H2 ambient, and (3) defect studies of the one-MeV electron irradiated GaAs LPE materials under different electron flux, fluence, and annealing conditions. The major findings and conclusions from this study are summarized as follows:

For the LEC grown Zn-doped InP, the main hole trap is due to the Ev + 0.52 eV hole trap with density of 1.5xE15 cm-3. Thermal annealing performed at 170 C showed a annealing rate of 0.025 per hour for this hole trap. In addition, CW laser annealing on this sample at 50 mW power level showed drastic reduction in defect density after a few minutes of laser annealing. Based on the annealing behavior of this defect, the origin of this defect may be due to the phosphorus vacancy related defect rather than any residual impurities. Additional study of the native defects in InP is currently being undertaken and, the results will be given in the next technical report.

Defect characterization in the LEC grown GaAs samples vs annealing temperature in hydrogen ambient for one hour has revealed some interesting findings. For annealing temperatures below 300 C, there are four electron traps with energies of Ec-0.35, 0.48, 0.61, and 0.76 eV and density in the mid 1E14 to mid 1xE15 cm-3 range.The density of these electron traps is decreased with increasing annealing temperature. When annealing temperature

increased to 500 °C, the defect sepctrum changed; the Ec-0.76 eV electron trap disappeared while Ec-0.83 eV (i.e., EL2) emerged in the DLTS spectrum. The present results are in accord with the observation by Day et al. in that they also observed the EL2 level in GaAs samples annealed at 700 to 800 C. In addition, our study of the defect profile for these electron traps indicated that these electron traps are bulk related defects, although the density of these defects tends to increase near the surface of the GaAs specimen. The decrease in the density of these electron traps with increasing annealing temperature also help to rule out the possibility that these defects are impurity related defects. Thus, it is adequate to state that these electron traps are most likely due to the Ga- vacancy or the antisite related defects. Photoluminescence measurements on these samples are currently being undertaken, and the results of this study may provide new information to the understanding of the origins of these defects.

Studies of deep level defects and their annealing behavior in one-MeV electron irradiated GaAs LPE layers have been carried out for different electron fluences, fluxes, and annealing conditions. From the results of analyzing DLTS and C-V data, it is concluded that: (1) one-MeV electron irradiation on GaAs fabricated by the infinite solution melt LPE technique will in general produce three to four electron traps and one to five hole traps depending on the fluence and the flux as well as annealing conditions; (2) defect density and number of deep level defects will increase with increasing electron fluence and flux; (3) increasing annealing temeperature and annealing time will reduce

the density and number of deep level traps induced by electron irradiation; (4) low temperature thermal annealing is effective in reducing the density of both electron and hole traps; (5) deep level defects observed in the undoped GaAs are somewhat different from those observed in the Sn-doped GaAs; (6) a comparison of the hole traps in the undoped GaAs irradiated at room temperature and at 200 C reveals that several shallow hole traps were annealed out for GaAs irradiated at 200 C, (7) a combined thermal and recombination enhanced annealing may be used to further reduce the defect density in the one-MeV electron irradiated GaAs LPE epitaxial layers.

VII. Publications and Conference Presentations Sponsored by the Current Grant

1. S. S. Li, C. Y. Lin, S. M. Bedair, and J. A. Hutchby, " Study of Grown-in Defects and Thermal Annealing Effects in Al0.3Ga0.7As and GaAs LPE Layers," J. of Electr. Mat.,Vol.11, No.2, pp.273-287 (1982).

2. P. C. Colter, C. W. Litton, D. C. Renolds, D. C. Look, P.W. Yu, S. S. Li, and W. L. Wang, "A Novel Ga/AsCl3/H2 reactors for Controlling Stochiometry in the Growth of Vapor Phase Epitaxial GaAs," Proc. of the International Symposium on the Semiconductor Growth Technology," vol.323, pp.328-335 (1982).

3. P.W. Yu, W. C. Mitchel, M. G. Mier, S. S. Li, and W. L. Wang, "Evidence of Intrinsic Double Acceptor in GaAs," Appl. Phys.Lett. Vol. 41(6), pp.532-535 (1982).

4. S. S. Li, W. L. Wang, P. C. Colter, and C. W. Litton," Study of Grown-in Deep-Level Defects vs Growth Parameters in GaAs Grown by VPE Technique," J. of Electronic Mat., vol.12,pp.223-234 (1983); paper presented at the 82' Electronic Materials Conference, June 23-25 (1982).

5. S. S. Li, W. L. Wang, R. Y. Loo, and W. P. Rahilly, " Study of Radiation Induced Defects and Annealing Effects in GaAs Solar Cells Irradiated by One-MeV electrons," Proc. of 16th IEEE Photovoltaic Specialists Conf., paper presented at the Conf., SanDiego,Ca., Sept. 28-Oct.1 (1982).

6. S. S. Li, W. L. Wang, R. Y. Loo, and W. P. Rahilly, "Study of Deep-Level Defects and Annealing effects in Undoped and Sn-doped GaAs irradiated by One-MeV Electrons," Solid State Elec. (1983).

7. S. S. Li, "Studies of Growth-in Deep-Level Defects and Transport Properties vs Growth Parameters in III-V Compound Semiconductors," Annual Technical Report, Air Force Office of Scientific Research grant No. AFOSR-81-0187A (1982).

VIII. References

1. R. M. Park, Electron Lett., vol.17, 669 (1981).
2. G. Bremond et al., Electron Lett., vol.17., 56 (1981).
3. P. Choudhury et al., Electron Lett., vol. 15, 247 (1979).
4. A. M. White, Electron Lett., Vol. 14, 40 (1980).
5. C. Wada et al., J. Appl. PHys., vol.51, 6158 (1981).
6. S. R. Macfee et al., J. Appl. Phys., vol.52, 6158 (1981).
7. Y. Yamazoe et al., J. Appl. Phys., vol. 20, 347 (1981).
8. A. Majerfeld et al., Appl. Phys. Lett., vol.33, 57 (1978).
9. O. E. Antypas et al., J. Appl. Phys., vol.4, 466 (1978).
10. S. Gaha, Solid State Electronics., vol. 20, 27 (1977).
11. M. Levinson, Appl. Phys. Lett., vol.40, 90 (1982).
12. B. W. Wessel et al., Semiconductor Growth Technology Symposium, SPIE., vol.223, 55 (1982).
13. M. Inuishi et al., Electron Lett., vol. 17, 685 (1981).
14. J. M. Kuo, Electron Lett. vol. 19, 41 (1982).
15. A. Sibbille, Appl. Phys. Lett., vol.41, 956 (1982).
16. M. Levinson et al., Electronic Materials Conference, (1982).
17. J. R. Knight, Solid State Electronics, vol.8, 1125 (1970).
18. R. C. Clark et al., Solid State Comm., vol.8, 1125 (1970).
19. J. J. Tietjen et al., J. Electro. Chem. Soc. vol. 122, 402 (1975).
20. M. Inuishi, J. Electro. Chem. Soc., vol.127, 2747 (1980).
21. B. W. Wessel, J. Electro. Chem. Soc., vol.122, 402 (1975).
22. A Majerfeld, Electron Lett., vol.11, 303 (1975).
23. J. L. Shay, Apply. Phys. Lett., vol.24, 192 (1974).
24. C. E. Wood, J. Appl. Phys., vol.49, 4954 (1978).

25. R. H. Bube, J. Appl. PPhys., vol. 49, 3397 (1978).

26. E. L. Benz et al., J. Elec. Materials, vol.19, 185 (1981).

27. K. Sakai and T. Ikoma, J. Appl. PPhys. vol.5, 165 (1974).

28. F.Hasegawa and A.Majerfeld, Electron Lett.vol.11,286 (1975).

29. C.I.Huang and S.S.Li,Solid Stat.Elec.,vol.16, 1481 (1973).

30. D.V.Lang and R.A. Logan,J. Elec.Mat., vol.4, 1053 (1975).

31. D. V. Lang and L.C.Kimberling,Inst.of Phys.Ser., 581 (1974).

32. A.Mircea and A. Mitonneau, Appl.Phys., vol.478,15 (1975).

33. H. Hasegawa and A. Majerfeld, Electron Lett.,11, 286 (1975).

34. A. Mitonneau et.al., Proc. of 6th Internat. Symp. on GaAs and Related Compounds, Inst. of Phys. London, 33a, (1977).

35. A. H. Kalma et al., IEEE Trans. on Nucleau Sciences NS-22, 6, 2277 (1977).

36. D. V. Lang, Inst. Phys. Conf.,ser., vol.31, 70 (1977).

37. A. H. Kalma and R. A. Berger, IEEE Trans. Nuclear Sciences, NS-19, 209 (1972).

38. J. A. Moore et al., Rad. Effects, vol.25, 49 (1975).

39. L. C. Kimerling et al., Apppl. Phys. Lett., 28, 297 (1976).

40. S.S. Li et al., IEEE Trans. Elec.Devices, ED-27,857 (1980).

41. D. V. Lang et al., Phys. Rev. B, vol.15, 4874 (1977).

42. C. M. Martin et al., Electron Lett., vol.13, 191 (1977).

43. R.D.Fairman et al., Inst. Phys. Conf.Ser., N45,134 (1977).

44. L.D. Aukerman and R.D. Graft, Phys. Rev., 127, 1576 (1962).

45. D. S. Day et al., J. Elec. Mat., vol.10, 445 (1981).

46. A. Y. Cho and H. C. Casey, Appl. Phys. Lett. 25, 288 (1974).

47. P. K. Bhattacharya et al., Appl. Phys. Lett., 36, 304 (1980).

48. F. Hasegawa and A. Majerfeld, Electron lett., 12, 52 (1976).

49. S. S. Li et al., Solid State Electronics, in press, (1983).

50. M. Jaros and S. Brand, PPhys. Rev.,B, 14, 4494 (1976).

51. S. G. Louie et al., Phys. Rev. B.13, 1654 (1976).

52. S. S. Li et al., Proc.16th IEEE Photovoltaic Specialists Conf.,(1982)

53. D. V. Lang, Inst. Phys. Conf. Ser., 31, 70 (1977).

54. L. W. Aukerman and R. D. Graft, Phys. Rev.B. vol.127, 1576 (1962).

55. H. Lefevre and M Schulz, Appl. Phys., 12, 45 (1977).

56. D. V. Lang et al. J. Appl. Phys., 47, 2558 (1976).

57. A. Ashby et al., Solid State Comm., 20, 61 (1976).

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